DEVICES FOR CONVERSION BETWEEN ANALOG QUANTITIES AND BINARY PULSE-CODED NUMBERS

by

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PREFACE

Section 2 of this paper describes the work of R. L. Sisson and Section 3 that of A. K. Susskind. Sections 1 and 4 were written jointly.

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ABSTRACT

When high-speed digital computers are used in information-processing systems, a need is created for devices which will convert analog quantities to binary pulse-coded numbers and binary numbers to analog quantities. Two specific devices to perform these conversions are developed in this thesis: a coder, which converts shaft positions into binary pulse-coded numbers, and a decoder, which converts binary pulse-coded numbers into voltage amplitudes.

The coder performs its conversion in three steps: (1) The shaft position is converted into a phase-modulated signal by a synchro control transformer. (2) The phase-modulated signal is converted to a pulse-position-modulated signal (PPM) by electronic clipping and peaking circuits. (3) The PPM signal is converted into a binary pulse-coded number through the use of a binary counter. Tests indicate that the coder will convert a shaft position into the corresponding binary number in 250 microseconds. Accuracy of 1 part in 360, sensitivity of 1 part in 1000, and good reliability are achieved. The coding system provides for electronic switching, so that the counter and other equipment required for step (3) above will be common to a large number of shafts.

The decoder is required to convert the binary number to a voltage amplitude and to "hold" that voltage amplitude. Since the computer is connected to a particular decoder only for short periods at irregular intervals, the "holding" feature is required in order to maintain the output of the decoder until new information is furnished by the computer. The

decoder developed here operates in four steps: (1) The binary number is converted to a PPM signal by the use of a binary counter. (2) The PPM signal is "held" by regenerating pulses in two special multivibrator circuits. (3) The "held" PPM signal is converted into a gate-width-modulated signal. (4) This signal is integrated by a low-pass filter to obtain a voltage amplitude which is proportional to the binary number to be decoded. The decoder also has provision for electronic switching, so that the equipment needed for step (1) can be common to a large number of output channels. The total decoding time depends on the output filter used; it is at least 150 microseconds. The decoder will "hold" the number for periods up to 5 hours. It has an accuracy of one part in 250.

As a test procedure, the coder was combined with the decoder by feeding the PPM signals from the former into the latter. This eliminates the binary counters and electronic switches, thus simplifying the test setup. Dynamic tests made with the combined systems showed that the accuracy and reliability under dynamic conditions are as good as that predicted from static tests, and that the frequency response of the system is determined entirely by the output filter in the decoder.

1.0 INTRODUCTION

In recent years, there has been a great deal of activity in the design and construction of large-scale, high-speed, digital computers. While these machines are powerful tools in the field of scientific computation and one could justify their existence on that basis alone, their use can be extended to broader fields, particularly to what has been aptly called "information-processing systems".[1] Indeed, it is in the field of information processing where the high speeds of modern computing machines are of the greatest advantage. When a scientific computation is to be carried out, the time allowed to obtain the result is not limited so narrowly as in control applications where the results of the computations must be made available to the system sufficiently early to be of benefit.

As an example of an information-processing system in which the use of a high-speed digital computer would be particularly effective, consider the control tower at an airport. Here information about the position of incoming planes, the identity of planes, flight plans, schedules, weather conditions, holding patterns, etc. is coordinated to achieve smooth, rapid, and safe flow of traffic. Present-day air-traffic-control systems are not fully mechanized, but rely heavily upon the judgment of human operators. These cannot assimilate the wealth of data which could be made available about the conditions in the vicinity of the airport. But a modern computer could, on the basis of all the available information, mechanize the control operation, thus leading to safer, more efficient, and more rapid handling of air traffic.

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1. Ref. 1

When a computer is to be used as part of an information-processing system, it becomes necessary to supply information about the conditions in the system to the input of the computer, and to furnish to the system the results of the computations in useful form. System variables are measured by devices which supply information in the form of shaft rotation, electrical voltage, or some other continuously varying quantity analogous to the measured condition. Similarly, the controlled system can accept information only in the form of analog quantities such as shaft rotation or electrical voltage. The computer, however, handles data in digital form. In "Whirlwind I", the large-scale, high-speed, digital computer now under development at the Servomechanisms Laboratory at M. I. T., quantities are handled in the form of binary numbers, i.e., numbers expressed as sums of powers of two. The numbers are formed electrically by pulse groups, with the presence of a pulse in a digit column representing the digit 1 and the absence of a pulse in a digit column representing the digit 0. Thus, when a computer such as "Whirlwind I" is to be used as part of an information-processing system, it becomes necessary, at the input to the computer, to convert analog quantities into binary pulse-coded numbers; at the output of the computer, binary pulse-coded numbers must be converted into analog quantities.

In Section 2 of this paper, a method of converting shaft positions into binary numbers is described. Section 3 discusses a method of converting binary numbers into electrical voltages. Section 4 describes the results obtained when the equipment of Section 2 was connected with that of Section 3.

The devices described here are designed to operate with only two types of analog quantities: electrical voltages and shaft rotations. In view of what has been said about information-processing systems, it might well be asked how other analog quantities (e.g., distance, velocity, force, pressure, etc.) might be converted into binary numbers. At the present time, it is proposed to convert these quantities into voltages or shaft rotations by the use of suitable transducers. Transducers also exist for the conversion between shaft rotation and voltage amplitude. Thus it must be borne in mind that the use of the devices to be described, although apparently restricted, is actually quite general.

2.0 CONVERSION OF SHAFT POSITIONS INTO BINARY PULSE-CODED NUMBERS

2.1 REQUIREMENTS TO BE MET

In systems where it is necessary to measure the position of shafts, these shafts are frequently located at some distance from the computing equipment. This condition means that the conversion from shaft position to pulse-coded binary number is usually accomplished in two steps. The first conversion is from shaft position to some form of electrical signal other than pulse-coded. The information is transmitted in this form from the shaft to the computer. Here a second conversion takes place from which one gets the binary pulse-coded number expressing the position of the shaft. (The terms first and second conversion, when used in this section, will have the meanings just given. Both steps are carried out by a unit which will be called a coder.)

The more obvious requirements imposed on the first conversion device are:

(1) mechanical and electrical stability.

(2) long life.

(3) ability to convert the shaft position into the desired type of electrical signal as accurately as possible.

Complex information-processing systems will contain many sources of information, all of which form inputs to the computer. In order to reduce the total amount of equipment, it is desirable to have as much as possible of the conversion equipment common to several inputs. Time

multiplexing is a useful technique for doing this. In time multiplexing, an electronic switch is used at the computer to select in sequence the signals arriving from the various shafts. The second conversion then takes place after the selector switch. By the use of this system, all the equipment following the switch is common to a large number of inputs, and the result is a reduction in the total amount of equipment required. Since time multiplexing is to be used, it is desirable that the signals coming from the shafts be easily selected by the electronic switch without the introduction of disturbing transients. This requirement, however, may conflict with the desirability of having the equipment at the shaft as simple as possible.

A most important requirement of the conversion system as a whole is that it be accurate. In many cases accuracies of 1/2 or 1% may be sufficient. However, in other cases a 16-digit binary number may be required, which is equivalent to an accuracy of 1 part in 32,768. Although we cannot expect a first conversion device to be more accurate than 1 part in 500, there is a system available which increases the effective accuracy of the over-all conversion without requiring more accuracy from the first conversion device itself.[1] Thus, even though accuracy should be as high as possible, reliability should not be sacrificed for accuracy.

Another requirement on the system is that the time needed to convert the shaft position into a binary pulse-coded number be as short as possible without sacrificing reliability or accuracy.

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1. Ref. 2., pp. 19-22

In the next few sections, we will discuss systems which accomplish the conversion and evaluate them in view of the requirements just presented.

2.2 HISTORY OF THE PROBLEM

2.21 Methods of Converting Shaft Positions to Electrical Signals (First Conversion)

There are several methods of converting the shaft position into an electrical signal. The first one which we shall mention converts directly to a binary pulse-coded number. The others do not.

A method of conversion which has actually been tried experimentally involves the use of a mechanical arrangement attached directly to the shaft.[1] Mechanical switches are incorporated in such a way that the position of the shaft actuates the switches according to the binary number which represents that position. The switches which are closed represent a 1 in the corresponding digit column, and those which are open a 0.

This system is simple and produces the binary number in the form of pulses directly. But the switch contacts are subject to wear, as are all mechanical switches, and hence require considerable maintenance. Furthermore, such mechanical arrangements are inherently slow, and this limits the number of times per second that the computer can sample the shaft position. (Sampling means measuring of the quantity at discrete intervals.) Also, high accuracy is difficult to obtain.

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1. Ref. 2., p. 3

The mechanical system can be replaced by attaching to the shaft a disc with alternating opaque and transparent areas and reading these areas with the aid of photoelectric cells.[1] Provision is also made for indicating the direction in which the shaft is turning. In this system, a pulse is developed each time the shaft rotates a certain incremental amount. These pulses are then used to drive a reversible binary counter which adds when pulses indicating clockwise motion are generated and subtracts when pulses indicating counterclockwise motion are generated. The number in the counter is then proportional to the shaft position at all times.

Systems which use a photoelectric device for the first conversion are usually very delicate and would require considerable maintenance. This particular system has the further disadvantage that each shaft requires a complete counting device; time multiplexing cannot be used. A large amount of equipment would be required wherever this system is used. It is, however, capable of high accuracy.

Another method for converting the position of the shaft into an electrical signal is based on the use of a variable-frequency oscillator.[2] For example, a capacitor which varies the frequency of an oscillator can be attached to the shaft. The output of the oscillator, probably in the form of a series of pulses, may then be used in various ways to obtain a binary number proportional to the repetition rate of the pulses and hence to the position of the shaft.

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1. Ref. 3.

2. Ref. 2., pp. 4-16

This system can be multiplexed, since the pulses from the oscillator may easily be switched by electronic means. The principle objection to a variable-frequency system is that a delicate electronic device, the oscillator, must be put at the location of the shafts, where it will be subject to vibration, weather conditions, etc. It is difficult to build a variable-frequency oscillator which will not drift and will not be sensitive to voltage changes, temperature drifts, and mechanical vibrations, even under laboratory conditions.

A direct way of changing the position of a shaft into an electrical amplitude is through the use of a potentiometer geared to a shaft.[1] This method is of some value if other inputs to the computer are in the form of electrical voltage variations, since then the same second conversion device may be used to convert the information from all the sources into binary numbers. On the other hand, potentiometers, having sliding contacts, wear out quickly and require constant maintenance. Furthermore, it is not easy to multiplex electrical signals whose amplitude variations constitute the information, since the electronic switching device may introduce errors in the nature of amplitude-varying transients. Also, potentiometers are inherently noisy and are difficult to build where 360° of rotation are required.

This brief survey of methods of conversion from shaft position to electrical signals indicates that it is desirable to develop a new type of first-conversion device which combines simplicity and ruggedness of the

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1. Ref. 2., p. 15

conversion device with a type of output signal which can be multiplexed. Such a conversion device will be described as part of this thesis.

2.22 Conversion of Electrical Signals to Binary Pulse-Coded Numbers (Second Conversion)

There remains to consider the problem of converting the signals arriving from the shaft locations into binary pulse-coded numbers. These signals may contain the information in various forms, but in several of the systems that have been proposed the signals are first converted into pairs of pulses the time interval between which is proportional to the given signal and then into a binary number by means of a binary counter. Since the binary counter will be an important element in this thesis, it will be described here in some detail.

A binary counter,[1] such as the one shown in Figure 1, consists of a chain of properly interconnected bi-stable circuits called flip-flops, which are shown in the figure by boxes marked FF. Each flip-flop has two vacuum tubes, so arranged that either one or the other is conducting, but not both. A pulse applied to the proper input will cause the previously conducting tube to be cut off and the previously non-conducting tube to conduct. Boxes marked GT represent gate tubes. These are coincidence tubes which can be cut off by either the control or suppressor grid. The suppressor grid is connected to the plate of the right-hand tube in the flip-flop. When that tube is cut off, the gate tube can pass a pulse applied to its control grid. Under that condition, we say that the flip-flop is in the 1 position. When the left-hand tube of the flip-flop is cut off, the gate tube cannot conduct and we say that the flip-flop is in the 0 position.

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1. Ref. 24.

The operation of the counter will now be explained. First, all the flip-flops are set to zero by pulsing the clear line. Then pulses are admitted to the input line. The first pulse entering the input will try to go through GT 1, but cannot do so since FF1 is set to 0. After a few tenths of a microsecond delay (action of box marked DE), this first input pulse will set FF1 to the 1 position. The next pulse on the input line first goes through gate tube 1 and sets the second flip-flop to the 1 position; it then resets the first flip-flop to the 0 position. This process continues, so that the third flip-flop is changed to a 1 when the fourth input pulse arrives, the fourth flip-flop when the eighth input arrives, etc. It will be seen that the state of the flip-flops will indicate in binary notation the number of pulses having entered.

The binary number held in the counter when all the input pulses have arrived may be read out to a set of lines (called the bus) consisting of one line for each digit. An extra set of gate tubes (the upper row in the figure) is required. The control grids of these gate tubes are all pulsed at the same time by a read pulse. A pulse will go out on each line for which the corresponding flip-flop holds a 1. Thus the binary counter can express the number of input pulses in binary pulse-coded form.

It will now be shown how a pulse-position modulated signal can be converted into a binary number by use of the counter, provided a fixed-frequency pulse generator (clock) and an auxiliary flip-flop and gate tube are available. A pulse-position modulated signal consists of control or reference pulses arriving at a fixed repetition rate, each followed by a

code or information pulse. The time interval between a control pulse and the following code pulse is proportional to the quantity being represented by the signal (e.g., the position of a shaft). The operation proceeds as follows. Refer to Figure 2. The binary counter is cleared just before a control pulse is to arrive. The control pulse sets the flip-flop (of Figure 2) to 1. This opens the gate tube which allows pulses from the fixed frequency oscillator to reach the counter. The code pulse returns the flip-flop to 0 and stops the flow of pulses. In this manner the number of pulses which have arrived at the counter is proportional to the length of time between the given control and code pulse. Since the binary number represented by the position of the stages in the counter is proportional to the number of pulses that have arrived from the fixed-frequency oscillator, the binary number is also proportional to the time between the control and code pulse. Just before the next control pulse arrives, the binary number may be read to the output lines, thus completing the conversion of the pulse-position modulated signal to a binary pulse-coded number.

As an example of the use of this method of converting the time interval between two pulses into a binary number, consider the question of coding the output of a d-c potentiometer attached to a shaft. The problem is one of converting a given voltage into a binary number. A direct method of doing this consists of developing a pulse-position modulated signal in the following way.[1] A linear sweep voltage is started at a definite time. The control pulse is generated at the same instant. A code pulse is developed at the instant when the voltage of the linear sweep

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1. Ref. 2., pp. 18-19

equals the voltage from the potentiometer divider. (It is assumed that the shaft position changes very little during the time of the sweep.) Thus the interval between the control pulse and the code pulse is proportional to the voltage output of the potentiometer. The control pulse and the code pulse are used to gate pulses at a fixed repetition rate into a binary counter as described above. A binary number is then obtained which is proportional to the shaft position.

The system to be developed in this thesis will use a binary counter to convert a pulse-position modulated signal into a binary number.

This history of methods of coding a shaft position is not complete. Other systems have been proposed which might be applicable to the conversion of shaft positions into binary pulse-coded numbers. Reference 4 describes several such ideas. None of these have been developed to any extent, however.

2.3 PRINCIPLES OF THE SYSTEM DEVELOPED HERE FOR CONVERTING A SHAFT POSITION TO A BINARY PULSE-CODED NUMBER

In this section the method by which a shaft position can be converted into a binary pulse-coded number is described. General criteria concerning accuracy, reliability, sensitivity, etc., are discussed.

2.31 Fundamental Operation

Three steps are required to develop a binary pulse-coded number which represents the position of the shaft. These are as follows: (1) By means of a synchro control-transformer the position of the shaft is transformed into a phase shift, so that as the shaft rotates a phase-modulated signal is developed. (2) This phase-modulated signal is transformed

electronically into a pulse-position modulated (PPM) signal. (3) The PPM signal is used to gate fixed-frequency pulses into a binary counter as described in Section 2.22. The binary pulse-coded number is then available by properly reading out of the counter. Figure 3 is the basic block diagram for this system. Let us examine each of these steps in more detail.

2.311 Converting Angular Position to Phase-Modulated Signals

The common type of synchro has a single-phase rotor and a three-phase (usually Y-wound) stator.[1] In the usual synchro systems the three voltages applied to the stator are in time phase. In the system being described, however, balanced three-phase voltages will be applied to the stator. As in the case of three-phase motors or generators, such voltages applied to the stator will create a rotating flux field in the air gap of the synchro; the rate of angular rotation in the two-pole arrangement that exists in the synchro[2] is equal to the applied frequency. The rotating flux field induces a sinusoidal voltage in the rotor winding. It can be seen that the phase of this sinusoid (called the rotor sinusoid) will change as the position of the shaft changes, and if the stator windings are properly distributed, the phase of the rotor sinusoid (in relation to some fixed reference sinusoid) will be directly proportional to the angular position of the shaft. We may take one of the three stator voltages as the reference phase.

The reason for choosing the control-transformer type of synchro is that it does have its windings so distributed that the linearity between phase-shift and angular position is maintained.[3]

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1. Ref. 5., pp. 439-444, and Ref. 7., pp. 12-2 to 12-26
2. Ref. 6., Chapt. 3, p. 26
3. Ref. 7., pp. 12-16 to 12-19

It can be seen immediately that the synchro is a rugged, stable device which may be placed on the shaft to convert its position into electrical signals (the rotor sinusoid). This system requires no auxiliary electronic equipment at the location of the shaft.

2.312 Converting Phase-Modulated Signals to Pulse-Position-Modulated Signals

In order to be able to handle the information contained in the incoming phase-modulated signals most efficiently in high-speed electronic circuits, it is necessary to convert them to a pulse-position-modulated (PPM) signal. The conversion is accomplished by developing 0.1 microsecond pulses that are accurately timed with the positive-going zero-crossings of the rotor and the reference sinusoids. This is accomplished by clipping and amplifying these sinusoids, and using the leading edge of the resulting square wave to trigger a pulse generator or peaker circuit. (The circuits which perform these operations are called the clipper-peakers.) The pulse generated from the reference sinusoid will be called the control or reference pulse, and that developed from the rotor sinusoid, the information or code pulse. It will be seen that the time interval between the control pulse and the succeeding information pulse will carry the information as to the exact position of the shaft. Figure 4 will make this clear.

2.313 Converting PPM Signals to Binary Numbers

The final conversion of the PPM signal to the binary pulse-coded number is carried out exactly in the manner described in Section 2.22.

In Figure 4 the "gate from the flip-flop" that is shown is the same gate developed by the flip-flop in Figure 2. The pulses to the

binary counter are also shown to illustrate the time relationships. The binary number read out of the counter for this case would be 101001101 (which is the binary equivalent of 333), where ones represent pulses and zeros no pulses.

2.314 The Complete System

The complete system is shown in Figure 3. Note how several shafts can be sampled by using an electronic switch. This diagram is considerably simplified, since it shows the counter always connected to the system. In general, the counter would be connected to the coders only when the computer is about to read a shaft position. The counter could be used for other purposes at other times.*

The system actually used in the thesis investigation, illustrated in block diagram form in Figure 5, has certain additions to the scheme described above which improve operation. These will now be discussed.

2.315 Synchronization of the Clock and Stator Frequencies

Consideration of the system used will show that the number developed for any given position of the shaft will change if either the repetition rate of the pulses from the clock-pulse generator or the frequency of the signal applied to the stator changes. The only case when this will not be true is if each of these frequencies changes in such a way as to cancel the effect of the other. Suppose a system could be arranged such that if the clock frequency increased the stator frequency would increase in proportion. Then if such an increase occurred the time

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* See Section 3.31

between the control and information pulse for the given position of the shaft would be smaller, since the stator frequency will have increased. But the number of pulses counted in that interval of time would be the same as before the frequency changed, because now there are more pulses per unit time as a result of the increase in clock-pulse frequency.

By synchronizing the pulse frequency and the stator frequency, the above result will be obtained; that is, the stator frequency will change in proportion to small changes in the clock frequency, and the number of pulses for a given position of the shaft will remain constant. This synchronization is obtained by the first five blocks of Figure 5. The clock-pulse frequency is divided by counting circuits to the proper stator frequency. The resulting pulse is used to generate a gate which is on for one-half the period of the desired stator sinusoid. This results in a square-wave signal at the stator frequency. The fundamental of the square-wave is extracted by filter circuits, giving the desired sinewave. Because the filter networks are not sharply tuned, slight changes in the clock frequency will result in proportional changes in the stator frequency.

2.316 Generation of the Three-Phase Voltages from a Single-Phase Voltage

Since the signal applied to the stator of the control-transformer must be three-phase, two R-C phase-shifting networks are used to shift the sinewave from the filter networks 120 and 240 degrees. The original sinewave and the two shifted waves form a three-phase signal to be applied to the stator.

2.317 Provision for Several Inputs

Figure 3 shows the arrangement used to allow the computer to measure the position of several shafts. The stators are all fed in parallel by the three-phase signal. Each rotor output feeds a separate clipper-peaker circuit which generates the pulse synchronized with the positive-going zero-crossing of the rotor sinusoid. An electronic switch is used to select the clipper-peaker output corresponding to the selected shaft. The pulse from the selected channel goes through the switch and becomes the code pulse. The control pulse and the selected code pulse then go to a counter to generate the binary number as discussed above. The selection switch is, of course, set up by the computer so that the proper channel will be selected.

In the thesis setup (Figure 5) we are concerned with only one shaft (at least to begin with); therefore, no provision is made for electronic switching.

2.32 Characteristics of This Coder

2.321 Time for Conversion (t_s)

Since this equipment is being designed for use with a high-speed computer, it is important that the time for conversion be as short as possible, so that the input equipment does not slow down the operation of the computer. The time for conversion may be defined in two ways. For the purposes of the following calculations the time for conversion (t_s) will be considered as the time between two successive control pulses, since — if the number is representing 360 degrees — this is the amount of time that must be allowed to let the counter reach its maximum count.

The time for conversion when defined this way is not exactly the same as the actual time interval required to send the number representing the shaft position to the computer after the computer calls for it, but it is closely related to this time.

In view of the above definition, the time for conversion is inversely proportional to the stator frequency. The interval between two successive control pulses is equal to the period of the stator simusoid. Thus we must consider whether the stator frequency can be chosen solely according to the desired time of conversion or whether other factors must be considered. Before discussing factors which enter into the choice of stator frequency, it is well to consider the order of magnitude of time of conversion required.

Suppose the computer is required to know the value of 50 inputs, some of which are shaft positions; it must deliver computational results to 50 outputs; and it requires about 25,000 microseconds of computing time between reading the inputs and delivering values to the outputs. Suppose further that a new value must be read from an input or delivered to an output 20 times per second in order to be able to follow the changes in the variables. (This whole situation is, of course, a simplification of any that might actually occur, but gives an order of magnitude. In Section 3.31 another way of looking at this problem is presented.) Our assumptions mean that we have 1/20 second to sample all the inputs, complete the computing, and furnish the results to the output channels. Therefore, all the terminal devices must be sampled in 1/20 second minus the computing

time of 25,000 microseconds, or in 25,000 microseconds. Since there are 100 terminal devices, we cannot spend more than 250 microseconds in each conversion process. This gives a fair idea of the timing required in one application of this type of coder. Note that this means the stator frequency should be 4 kc or higher.

The actual interval between the time when a computer asks (by means of a special pulse) for the position of shaft x and the time that this information is available (in the form of a binary pulse-coded number) to the computer is not in general equal to t_s. The time required to read a shaft will be designated as t_r. In general, the exact magnitude of t_r will depend on the way the computer is set up. Usually, the following steps must be taken:

(1) The computer needs to know a shaft position. It sets up a switching and control system which will (a) indicate that a shaft position is to be read and make electronically the necessary interconnections, (b) indicate which shaft position is to be read, and (c) clear the binary counter. This all requires a very short time (of the order of 10 microseconds).

(2) Nothing happens now until a control pulse arrives. The time at which the computer asks for the information is not usually synchronized with the control pulses (although it can be), so that it requires a time equal to $t_s/2$ on the average before a control pulse arrives. This time may be as long as t_s.

(3) Clock pulses then pass on to the counter and set it to the proper number. The information pulse may be used not only

to shut off the flow of pulses to the counter, but also to indicate to the computer that the number in the counter is ready to be read. This step may take as long as t_s if the position is near 360°, but if the shaft is turning in a completely random fashion it will take $t_s/2$ on the average.

Adding the times required for all of these steps, we see that t_r may be as long as $2t_s$ (plus a small amount of time for step one and for reading out of the counter). On the average, however, the time to read out will be equal to t_s (plus the same small amount of time). Thus we are justified in using t_s as a criterion in determining how much time will be taken in reading a shaft position.

Some reduction in the time to read out can be obtained if computing continues while the counter is being set. This involves some complications in programming, however.

2.322 Sensitivity

To get back to the question of what other factors influence the choice of stator frequency, consider the question of sensitivity. Sensitivity is defined as the smallest change in shaft position that will cause a change in the binary number at the output. For instance, a sensitivity of 1 part in 1000 (or 1/1000) would mean that a change in shaft position of 1/1000 revolution (or 0.36 degrees) would cause a change of one unit in the binary number. Disregarding other factors, the sensitivity should be as small a part of a revolution as possible.

Consideration will show that the sensitivity depends on two factors, (1) the stator frequency, and (2) the clock frequency. In fact,

if we let S denote the sensitivity (expressed as a fraction of a revolution), f_c denote clock frequency, and f_s stator frequency then $S = \frac{f_s}{f_c}$. As an example, suppose f_c is 10 mc and f_s is 5 kc. The sensitivity would then be 1/2000. In one period of the stator sinusoid there will be a maximum of 2000 clock pulses. Providing the rest of the system is sufficiently sensitive, the counter could detect the presence of one additional clock pulse, or of 1/2000 part of the maximum input (one revolution).

We noted in Section 2.321 that the time for conversion (t_s) is inversely proportional to frequency f_s. Thus $S = \frac{1}{f_c t_s}$ and we see that for a given f_c we can decrease the time for conversion only by impairing sensitivity, or, conversely, sensitivity may be improved by lengthening the time required for the conversion. Note further that we gain both ways if we increase the clock frequency; that is, time of conversion may be decreased without increasing S. The maximum clock frequency that can be used is set by other considerations, the most important being that the counter and other equipment will not operate at excessively high clock frequencies. In practical application, sensitivity and time for conversion are given, and the clock and stator frequencies are chosen to meet these requirements, if possible.

2.323 Accuracy

Accuracy must be distinguished from sensitivity, although the two are related. Sensitivity measures the ability of the device to indicate small changes in the input. Accuracy is the relation between the input and the output. For a given output, one can say that the input is actually

within x parts of a revolution of the value of the output. This figure x is then a measure of accuracy, and should, of course, be as small as possible. For many uses accuracies of the order of 1/360 (that is 1.0 degrees) are sufficient. One might ask at this point if it is ever necessary to have a sensitivity better than the accuracy, but actually there are times when it is more important to indicate a change in the variable than to know its exact value. This is especially true where the device is part of a feedback loop. Of course, the same things that cause inaccuracy could also cause insensitivity, but that is not true of this system.

There are two types of inaccuracy that may occur in this system. There is, first of all, the relative error or the error which is a function of the angle. That is, we may suppose that the system is adjusted so that an angle of zero degrees produces the number zero in the output. If there were no inaccuracy, then there would be a linear relation between the angle and the number going to the computer. Any deviation from this linear relation will be an inaccuracy. Often this type of error is cyclical, that is the numbers vary from those given by the linear relation in a cyclical manner when plotted as a function of angle. This type of error is called relative since it will occur regardless of what number is chosen to represent zero degrees.

The second type of inaccuracy is due to the fact that the number representing zero changes with time, temperature, voltages, frequency or any other parameter. Of course, as the number representing zero degrees changes, all the other numbers change in proportion so that the relation between the number output and the angle is still linear (assuming no

relative error). Nevertheless, this type of inaccuracy is very important. The computer must know not only the relation between the actual angle and the numbers it receives, but must also know which number represents zero position. Once the computer has these constants, they must not change,* since if there is a drift in zero position the computer will misinterpret the numbers it receives. We will consider the problem of zeroing and zero drift in Section 2.3232. First, we will discuss sources of relative error.

2.3231 Relative Errors

Inspection of the block diagram will show that the only elements whose operation is affected by a change in the shaft position are the synchro, the flip-flop and gate tube at the input to the counter, and the counter. All the other equipment operates independently of shaft position. For the purposes of this thesis we are assuming that the flip-flops, gate tubes, and the counter operate correctly. (This means that any jitter in the timing involved is less than 0.2 microseconds and hence less than the time between two clock pulses.) Thus the principle relative inaccuracies must come from the control-transformer itself.

Errors in the control-transformer come from three sources: (1) imperfect windings, (2) imperfect balance of the three-phase stator voltages, and (3) harmonics either in the stator voltages or induced by the magnetic circuit itself. The control-transformer used has windings that are precision-made, and the error due to imperfections in the windings is believed to be less than 1/5 degree. The error caused by unbalance of the three-phase can also be made quite small by careful adjustments using

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* This may not always be true since it is possible to have the computer periodically check its zero against the actual zero position of the shaft.

methods described later. These errors are not negligible, however. The error due to harmonics is quite important, since it is not easily controlled, and is believed to be a major source of inaccuracy. We will consider this problem later (Section 2.5223).

The aim in the development of this device is to get accuracies of about 1/360 or about 1 degree. This should be attained with good stability so that readjustments are required no oftener than once a day. We assume that if greater degrees of accuracy are required, multiple-speed systems will be used (see Section 2.63).

2.3232 Zeroing and Zero Drift

As we have mentioned previously, the computer must know which number represents the zero (that is the reference) position of the shaft. Usually, of course, this number will be zero. We have also implied that this relation between zeros should be constant with time. First, however, let us see how we would adjust the system so that the zeros coincide.

First, we could just take the system without adjustment, so that some arbitrary number represents the reference position, and then make allowance for this fact in the program used by the computer in solving the problem. This is not desirable in many cases, however, since it may increase the computing time required. It also is inconvenient for the persons writing the program since the reference number for each shaft would be different.

The next thing that could be done is to mechanically adjust the control-transformer position until the zeros did coincide. This method

would probably be used after installation, and can also be used if any later adjustments are needed. Another way to vary the number representing a given shaft position would be to introduce a phase-shift in the rotor output. This is equivalent to advancing or delaying the code pulse in respect to the control pulse, so that the two pulses can be made to coincide for the shaft position which is to be the reference position. It is possible to delay the code pulses themselves, but in general it is much easier to get phase shifts which are equivalent to long delays, than to get the delays. Using the phase-shifting arrangement allows one to let the number zero represent any particular shaft position at any time.

This last system of zeroing suggests a source of zero inaccuracy. We must be sure that the phase (or more generally the time relation) between the reference sinusoid (or reference pulse) and the rotor sinusoid (or the associated code pulse) does not change except as a function of shaft angle. Let us consider which components in the system might give rise to zero drifts. There are two. First, consider a change in the exact part of the cycle at which one of the clipper-peakers produces its pulse. If either of the clipper-peakers changes in such a way that the pulse is produced before or after the zero-crossing of the sinewave, this will be equivalent to introducing an advance or delay of the control or information pulse (whichever the case may be). This would in turn cause a change in the zero position. It is believed that the clipper-peaker circuits are so designed that this type of zero drift will be negligible, if voltages are reasonably well regulated. The second source of this type

of error is in any coupling networks used, either in the rotor circuit to set the zero position as described above, or in the coupling circuits within the clipper-peakers. These circuits, being passive, are not likely to give trouble by drifting with time, but the phase shift could change as a function of frequency, and we have seen (Section 2.315) that, because the system is synchronized, the frequency need not be constant. This effect is actually made negligible in the internal coupling circuits by making the phase vs. frequency characteristics flat over the frequency range in question. (That is, these circuits have the proper frequency response in the region of interest.) However, any circuit placed after the rotor for the purpose of adjusting the zero position or for other reasons may introduce a considerable phase shift as a function of frequency unless special care is taken in the design of the circuit. In general, it is best to adjust the zero position by mechanical means.

If the circuits for this system are all properly designed, the zero adjustment, once set, should be constant in spite of reasonable variations in frequency, voltages or other parameters.

2.324 Ultimate Values for Time of Conversion and Sensitivity

It is interesting to consider the best performance that can be obtained from this system of conversion between shaft position and binary pulse-coded numbers. Probably the ultimate over-all limitation is how fast the counter can count. Counters available today can be made to operate with pulses occurring at 5 mc. A 10 mc counter has been constructed,[1]

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1. Ref. 8

and it seems possible that if all the techniques known in the art of electronics were applied, a 15 mc counter could be developed. This last figure will be used as one upper bound on performance.

The other important limitation is that the accuracy is limited by the device used to convert the shaft position into a phase-modulated signal (the first conversion device). This device must be mechanical, and it is probably not possible to make such devices with an accuracy of greater than 1/500 revolution. It does not seem likely that the sensitivity will ever have to be more than 1/4 the accuracy, so that S = 1/2000 can be considered another upper bound.

These two bounds lead to the conclusion that, if we used the maximum sensitivity of 1/2000, then the time for conversion would be about 133 microseconds. The stator frequency would be 7.5 kc.

One might also ask how high the stator frequency may be made. This question is especially important if we wish to reduce the conversion time. For instance, if the conversion time is reduced to 20 microseconds (by allowing a sensitivity of 1/300, which may be sufficient in many cases) the stator frequency would have to be 50 kc which seems rather high for an electro-mechanical device such as the control-transformer. Experimental evidence proves, in fact, that synchro devices cannot be used at frequencies above 20 kc.[1] This is not a real limitation, however, since from 20 kc up to over 100 kc a capacitor-type phase-shifter or an air-core control-transformer could be used. Thus we see that conversion times of 20 microseconds combined with a sensitivity of 1/300 are not infeasible. It should

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1. Ref. 5., p. 497

be mentioned that capacitor phase-shifters are not capable of the high sensitivity of the synchro.[1] But capacitor phase-shifters would probably only be used where short conversion times are more important than sensitivity. Also, capacitive devices are not as rugged as synchros and are much more sensitive to variations in the capacitance of the loads to which they are coupled. Hence, they should only be used where the short conversion time (less than 50 microseconds) is absolutely necessary. Information on air core synchros does not seem to be readily available, but they seem to be worth investigating for high-frequency work, especially since voltage levels in this system can be low. For the purposes of this thesis the iron-core synchro is entirely satisfactory.

2.325 Parameters Chosen for the Thesis Investigation

The frequencies for the system to be tested in the thesis were chosen in the following manner. A consideration of the possible uses to which this system might be put in the near future indicated that a conversion time of 250 microseconds should be satisfactory, and that a sensitivity of about 1/1000 of a revolution would be required. This leads immediately to the choice of a stator frequency of 4 kc and a clock frequency of 4 mc. Fortunately, the electronic equipment on hand will function at 4 mc, and, as we have said, 4 kc is well within the useful range of frequencies of a control transformer. Also, this system will operate satisfactorily with the decoding system described in Section 3.

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1. Ref. 5., pp. 492-496

If this coder is to be employed in systems with different requirements, changes in the direction of a shorter conversion time and less sensitivity will probably be required. This can be accomplished by increasing the stator frequency.

2.326 Advantages of the System Developed in This Thesis

To summarize, the system being described has the following advantages:

(1) The first conversion device (a synchro control-transformer) is very stable and rugged, and requires practically no special maintenance. It requires only one set of three-phase voltages of low amplitude (less than 10 V) and no direct potentials such as vacuum-tube circuits require.

(2) All of the electronic equipment that might require special adjustment may be put in the same place as the computer, where it may easily be checked and serviced.

(3) Accuracies of the order of 1° of shaft rotation (one part in 360) are obtained.

(4) The system may be used to advantage in radar applications, where the range data is already pulse-position modulated data, and may be converted into binary numbers in the same counter that is used to convert the shaft position data.

(5) The sampling rate may be high if desired, so that fast moving shafts may be measured.

(6) Time of conversion may be made very short. In the system developed it is 250 microseconds, but can be shorter.

2.4 DESCRIPTION OF THE INDIVIDUAL UNITS USED IN THE THESIS INVESTIGATION

In this section, we describe each of the units that are used in the coding system.

By way of summary, we may list the component units required to complete this system. The exact descriptions of the units will then be presented in order.

(1) 4 mc Pulse Generator (Clock)

(2) Frequency Divider (3 cascaded units are required to obtain 1000/1 division)

(3) Gate Generator

(4) Filters and a Phase-Shifting System

(5) Control Transformer

(6) Clipper-Peakers (for developing pulses synchronized with the positive-going zero crossing of a sinewave)

(7) Electronic Switch

(8) Counter

(9) Flip-Flops and Gate Tubes

2.41 The Clock-Pulse Generator

The clock pulse generator produces pulses at a repetition rate of approximately 4 megacycles. The clock pulses are standard pulses for Whirlwind equipment. These pulses are approximately half-sinusoids, 0.1 microsecond long, and at least 15 volts in amplitude.

The clock-pulse generator actually used is one of a number of standard test units developed by Project Whirlwind to facilitate the testing of equipment. The detailed description of these standard test units is available in Project Whirlwind reports.[1] We will not, therefore, give

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1. Ref. 9 and Ref. 17

details of any of the units used in this thesis which are also standard Whirlwind test-equipment units.

The clock-pulse generator consists of a sinewave oscillator whose frequency is variable over a range from about 200 kilocycles to 5 megacycles. The output of this oscillator is clipped and amplified and fed to an RLC peaker which produces the standard pulses at the same frequency as that of the oscillator. As we have said before, in the system for converting shaft position into a binary pulse coded number, the frequency is set to 4 megacycles.

2.42 The Dividers and Pulse Standardizer

Following the flow of the signal as presented in the block diagram (Figure 5) we next come to a 1000-to-1 divider stage. This stage consists of three 10-to-1 dividers. These units are commercial decade dividers built by General Electric called Decade Scaling Unit Type YYZ-1.[1] Each 10-to-1 divider consists of a flip-flop or a scale-of-two circuit followed by a ring counter set up as a scale-of-five circuit. This arrangement gives a total division of 10 to 1, and is considerably more reliable than the more common multivibrator frequency-divider since all tubes operate on an "on or off" basis. According to the manufacturer, these units are capable of accepting and counting pulses at a continuous rate of up to 5 megacycles, and therefore should be perfectly satisfactory for our purposes. The output pulse is a positive pulse approximately 1 microsecond wide and 40 volts in amplitude. Since this is not a standard

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1. Ref. 10

0.1 microsecond pulse, a pulse standardizer is used to develop a pulse to trigger the gate generator which follows the divider. The pulse standardizer[1] is an RLC peaker followed by an amplifier. Figure 6a shows the clock pulses, and 6b the output of the first dividers. The output of the last divider is of the same shape and differs only in frequency.

2.43 The Gate Generator

The output of the divider occurs at a 4 kilocycle rate. It is then necessary to generate a 4 kilocycle sinusoid. It was decided that the easiest method of doing this, considering the equipment available, was to generate gates of 4 kc repetition rate and then filter out the fundamental from the resulting square wave. The gate generator is one of the standard Whirlwind test equipment units. It consists essentially of a one-shot multivibrator whose "on" period may be varied from approximately 1/2 microsecond to as long as 2500 microseconds.[2] (A delayed pulse generated from the trailing edge of the gate may also be obtained from a gate and delay unit.) It will be seen that for our purposes the gate length should be set to 125 microseconds. The output of this gate generator will then be a square wave which is positive for 125 microseconds and negative for 125 microseconds, and thus has a fundamental frequency of 4 kilocycles. This is shown in Figure 6c. Since the gate is triggered on by the pulse from the 1000 to 1 divider, it is synchronized with the 4 megacycle clock pulses. The amplitude of this gate is about 40 volts.

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1. Ref. 11
2. Ref. 12

2.44 The Filters and Phase-Shifting Networks

As we have said, this 4 kilocycle square wave must first be filtered so that only the fundamental frequency remains. We must then take the resulting sinewave and shift its phase both 120 and 240 degrees, so that we will have a three-phase signal at 4 kilocycles. Refer to Figure 7. It was found that two π-section low-pass filters with a cutoff at about 4300 cycles per second were required to isolate the fundamental frequency of the square wave. The first filter[1] (an m-derived π-section) is placed at the input to the amplifier (V_1 in Figure 7). The second filter[1] (a constant-k π-section) is placed in the output of that stage. The purpose of V_1 is to drive the transformer T_1, and to compensate for the losses in the filters. The wave forms of the output of the gate generator are shown in Figure 6c, and the signal after the first filter in Figure 8a. The signal after the second filter is very nearly a pure sinewave. The output of the transformer is arranged in a push-pull fashion and is followed by two R-C phase-shifting networks. One R-C network shifts the phase by $+120^\circ$ and the other by -120°, neither introducing any appreciable change in amplitude. The conditions for adjusting R_1 and R_2 to give 120° phase shifts are:[2]

$$\frac{1}{\omega C_2} = \sqrt{3} R_2$$

$$\frac{1}{\omega C_1} = \frac{R_1}{\sqrt{3}}$$

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1. Ref. 13., p. 132
2. Ref. 5., p. 139

A method of making these adjustments is discussed in Section 2.523. By means of the phase-shift networks, we have 3 sinusoids, all of approximately the same amplitude, but each 120 degrees out of phase with the others. (All three are shown simultaneously in Figure 8b. Note that in this figure, the amplitude of one phase is slightly higher than of the other two. This undesirable situation was later corrected by placing a 3500 ohm resistor across the plate load (2000-ohm resistor) of V_2 to reduce the gain in that stage slightly.) These three sinusoids are then applied to the grids of tubes V_2, V_3, and V_4 in Figure 7. These tubes prevent the phase-shifting networks from being loaded by the low impedance of the control-transformer stator. The phase-shift networks would introduce undesirable amplitude changes if not operated into a very high impedance. The outputs of V_2, V_3, and V_4 are coupled to the stator of the control-transformer by means of matching transformers so that the proper impedance matching conditions will be met. The impedance of a stator lead to ground is approximately 600 ohms at 4 kilocycles. The plate of the tubes is made to look into approximately 20,000 ohms due to the step-down winding of these matching transformers.

The 0.5 microfarad capacitors across the stator windings were used to help tune the windings. It was later found that they are unnecessary, and they were removed. The purpose of the rotor filter drawn in Figure 7 will be discussed in Section 2.523.

Type 6AS7 tubes are used throughout this circuit because that type will handle the large grid signals which exist. The output of the 1st low-pass filter is approximately 32 volts peak to peak (see Figure 8a),

and since we require this signal to be amplified in a linear fashion, the tube must be able to handle these large grid swings. The 6AS7 tube was found to be the best one available for this purpose. Each stage has a gain of approximately 2.

2.441 The Derivation of the Control Pulse

The control pulse is developed from one of the stator sinusoids by a clipper-peaker circuit. The only unusual point here is that the reference sinusoid is taken from the primary side of the transformer which feeds the stator (rather than directly from the stator) as shown in Figure 7. This was done because (1) the amplitude of the signal on the primary side is larger and the clipper-peaker operates better with larger inputs, and (2) because when a filter is placed in the rotor output to remove harmonics (Section 2.523) the stator waveform is affected by the reaction of the armature flux field on the stator windings. This distortion varies the time of the zero-crossing of the reference phase as the rotor is turned; therefore, it would introduce considerable error into the system. It was found that on the primary side of the transformers the waveform was not affected by the armature reaction, and connecting the clipper-peaker at this point worked very well. The problem of distortion due to armature reactions was later eliminated by a method described in Section 2.526, but the 2nd clipper-peaker was still fed from the primary of the transformer because of the higher amplitude.

This change in the point from which the control pulse is derived could not be made if the transformer introduced a phase shift as a function of frequency and hence a zero error. There is apparently no such effect, however, and no trouble was experienced in obtaining the desired accuracy.

2.45 The Control Transformer

Obviously the control-transformer is a most important unit in this conversion system. Some time was spent, therefore, in examining the characteristics of the various control-transformers available in terms of accuracy, ruggedness, reliability, and size. The unit finally chosen was the Autosyn Type AY101D made by Eclipse Pioneer, a division of the Bendix Aviation Corporation. This synchro is a 400 cycle device which normally requires a rotor excitation of 26 volts. It has a single-phase rotor and a 3-phase Y-connected stator. According to the manufacturer, the accuracy spread of this unit when used in a synchro follow-up system as a receiver should be less than 0.4 degrees.

It will be noted that we intend to use the control-transformer slightly differently than in the manner for which it was originally designed. In the first place, we are going to apply 3-phase signals to the stator, and in the second place we are going to operate at 4 kilocycles instead of 400 cycles. Preliminary tests were made on this control-transformer which indicate that the resonant frequency of the windings is well above 30 kilocycles, and that operation at frequencies as high as 20 kilocycles could be obtained. Certainly no trouble was experienced at 4 kilocycles. The fact that we are applying 3-phase to the stator rather than 3 single-phase voltages has no detrimental effects on the unit.

In this thesis the line-to-line stator voltage was about 3.2 volts, and the output from the rotor about 5.4 volts rms. These amplitudes could be higher if needed without damaging the control-transformer, but no such need arose in our work.

2.46 The Clipper-Peakers

The clipper-peaker is the second type of circuit which was designed specifically for this application. There are two used in the thesis, the first for the control-pulse and the second for the information pulse. They are required to develop a standard pulse accurately synchronized with the positive-going zero-crossing of a sinewave input. There are two principle ways for so developing a pulse: (1) by means of regenerative amplifiers[1] which, because of their non-linear regenerative nature, give a very large amplification for a small range about some particular value of the input, and (2) by means of clipping stages followed by amplifying stages.

Two different types of regenerative amplifiers were tried in an attempt to produce either a pulse or a sharply rising wave-front accurately synchronized with the zero-crossing of a sinewave. Although these circuits worked, they had two principle drawbacks. These were (1) they tended to oscillate; that is, they produced an output even though there was no input (oscillations occurred because of the large amount of regeneration required to get sufficient rise times) and (2) the exact point in the sinewave at which the pulse (or steeply rising wave-front) was developed varied. In other words, the pulse not always developed at exactly the zero-crossing of the sinewave. This timing was especially sensitive to variations in certain voltages.

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1. Ref. 14 and 15 and Ref. 5, pp. 349-50

Since the operation of the whole conversion system depends upon being able to develop pulses synchronized with the zero-crossings without introducing any unnecessary time delays or time jitter, regenerative circuits were rejected and it was decided to use the second method. In this method the sinewave is clipped by means of diodes and then amplified, and this process is repeated several times so that the output is a square wave whose rise and fall are accurately timed with the zero-crossings of the sinewave. It was found that this system works very well and does not require many more tubes than the regenerative system. The clipping method has the advantage that it was quite insensitive to voltage changes and to deterioration of the tubes.

Figure 9 shows the details of the clipper-peaker circuit finally used. Note that clipping is accomplished by means of crystal diodes[1] (Type D359). These diodes are entirely as effective as high-vacuum diodes in this application. Crystals also have a longer useful life and are smaller in size. Referring to the circuit diagram in Figure 9, we see that the sinusoid is clipped immediately as it enters the circuit. The 10 k resistor (R_1) provides an impedance against which the clipping action may take place. The D359 crystals used for this clipping have characteristics which are shown in Figure 10. Note that the forward resistance is less than 50 ohms except for voltages less than 0.5 volt, and that back resistance is more than 150,000 ohms. Since the two diodes are essentially

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1. Ref. 16

in series with R_1, when either diode has a voltage of more than 0.5 volt across it in the forward direction, the signal is reduced by a factor of about 50/10000 or .005, while for a 1.0 volt range about zero input, neither crystal is a very low resistance and the signal is reduced by a much lower factor. For example, at 0.1 volt the signal is reduced by about only .1 and nearer zero by even less. The clipping action of the two diodes connected as shown is thus quite effective. Figure 11a shows the output of the rotor for two different shaft positions. This sinewave is also the input to the clipper-peaker. Figure 11b shows the voltage across the two diodes. This signal is applied to a stage which is simply a class-A pentode-amplifier stage except that the load resistance is non-linear, because of the clipping action in the grid circuit of the next stage. Here again the crystals are used for clipping. Note that a bias of approximately two volts is applied to the crystals (by resistors R_2 and R_3) so that the clipping action does not occur until the signal is greater than 2 or less than -2 volts. The signal at this point is shown in Figure 11c.

The final amplifier stage (V_2 in Figure 9) is unusual in that it has an inductive plate impedance. The reason for this is as follows:

In this stage the rise time of the plate wave is limited by the relatively slow fall of the grid waveform rather than by the frequency response limitations of the stage (even with a high impedance load). The grid falls at about 1.6 volts per microsecond whereas the tube will amplify signals falling as fast as 10 volts per microsecond. Thus, in order to get the slope of the wave-front as large as possible it is desirable to make the stage gain as large as possible. This can be done

by putting a large impedance in the plate circuit. A large resistor would be satisfactory except that it requires high d-c voltages. Therefore, an inductor is used (L_1), since it has a high impedance during the rise time, which is the only part of the waveform we are interested in.

The purpose of the crystals across the inductor is discussed after we consider the way in which the peaker operates.

Figure 12a shows the waveform at the plate of V_2. The rise time of the positive pulses is about 50 volts per microsecond. The waveform is not flat across the top, but is a pulse because the inductance does not remain a high impedance after the initial sharp fall on the grid. Since we are only interested in the plate rise, however, this effect is not important.

A gas-tube peaker (V_3) is used since it develops a large amplitude output at a low impedance level. Thus no buffer amplifier is required to drive a cable, as would be the case if an R-L-C peaker had been used. When the peaker tube fires, the plate to ground capacitance (C_2) discharges. Since it takes about 200 microseconds for this capacitor to recharge (through R_4), the tube fires only once. The inductances ($L_{2,3}$) and C_2 are a pulse forming circuit. This circuit causes the output pulse across a 100 ohm cathode resistor to be 0.1 microsecond long. The output pulse, shown in Figure 13b, is about 100 volts in amplitude. (The pulse in Figure 13b appears slanted because the pairs of deflection plates in the oscilloscope were not exactly perpendicular.)

In considering the coupling of the plate waveform of V_2 to the grid of the peaker tube (V_3), it must be remembered that when the peaker

tube conducts its grid draws current of the order of 2-3 ma. In order that this current does not build up a bias on the capacitors in the coupling circuit, the time constants must be kept short. It will be seen that the time constant formed by C_1 and R_5 and R_6 in parallel is about 10 microseconds. (Refer to Figure 9.) The minimum interval between two successive firings of the peaker tube is more than 200 microseconds, so that any charge built up on C_1 by grid current leaks off before the next firing. Therefore, the grid is kept at -9 volts obtained from the voltage division in R_5 and R_6. The tube (V_3) will fire with a grid voltage of about -4 volts, and thus fires during the sharp rise applied to the grid. The differentiating action of the short-time-constant coupling is only an incidental effect in this circuit.

Figure 12b shows the rise on the grid of the peaker just before and after the tube fires. Note that the slope of the waveform before the tube fires is about 50 volts per microsecond. (See also Figure 12c, which shows the grid waveform with the peaker tube removed so that the effects of grid current are eliminated.) The maximum variation in the exact firing voltage of the thyratron (V_3) is $\pm$ 2 volts.[1] (This includes the effects of aging, temperature variations, etc.) Since we want the jitter due such variations to be less than 0.1 microseconds, the slope of the waveform should be at least 4 volts per 0.1 microsecond or 40 volts per microsecond. The existing rate of rise is therefore sufficient.

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1. Ref. 18

The crystal diodes connected across the inductor (L_1) are for the purpose of clipping the negative going pulses. These pulses are not, in themselves, disadvantageous, but if they are allowed to remain at full amplitude, they are followed by a large positive overshoot.[1] This positive signal applied to the peaker grid was found to be enough to re-trigger the peaker tube, which of course is highly undesirable. (The peaker should fire only on the positive going pulse which is developed when the grid of V_2 goes negative.) The diodes effectively damp out the negative pulse and hence the overshoot which would normally follow it.

These clipping diodes tend to reduce the rise time of the positive pulse since the impedance in the plate is limited by the back resistance of the crystals, rather than by the inductor. However, the rise time is still sufficient in this case. Two crystals are used in order that the inverse voltage rating for this type of crystal will not be exceeded. The 220 ohm resistor helps to limit the peak forward current through the crystals to a safe value.

Figures 12a and 13a show the effect of the clipping action on the overshoot. Note that in Figure 13a the peaker would fire at both "A" and "B", "B" being the time of the unwanted overshoot. With the damping diodes, firing occurs only at "A", as shown in Figure 12a. Figure 13c shows the output of the peaker superimposed on the input to the clipper-peaker circuit. Time delays in the test equipment are probably the principle reason why the pulse does not appear to occur exactly at the zero-crossing of the sinewave.

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1. Ref. 19., pp. 127-8

2.47 The Electronic Switch

In this thesis we are assuming that components such as the electronic switch[1] are available. No attempt was made to construct a switching device, and in fact attention was focused mainly on the operation of the system with only one shaft.

Because of the placement of clipper-peakers before the switch (see Figure 3), only pulses need be gated by the switch, and this is easily accomplished. It might seem at first that a considerable saving could be made in the number of tubes required if the switch were fed directly by the rotor outputs, because then a single clipper-peaker following the switch would serve for all shafts, thus reducing the number of clipper-peakers required. This method would mean, however, that the switch would have to select sinewaves. A survey of methods of selecting sinewaves[2] showed that at least two and probably more tubes per input from a shaft would be required (in addition to the usual gate tubes in the switch) in order that the sinewaves would not be distorted by the gating action of the switch, and in order that the switching time be small compared to the conversion time of the system. Since the clipper-peaker has only three tubes, the actual net saving in tubes would be small, if any.

(The only other problem in operating with more than one shaft position is in driving all the stators. The problems of power and of impedance matching are trivial. The important question is whether the phase-balancing adjustments made for one stator will be correct for the

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1. Ref. 20
2. Ref. 2., p. 18

others. Since the control-transformers used are precision wound, the adjustment should hold for a number of units, providing that the reaction of the rotor current on the stator waveform is sufficiently small. This problem is discussed further in Section 2.526.)

2.48 The Counter

The counter is another element in the system which we assume can be obtained. The only requirement on it is that it be able to count pulses at the required rate (4 mc in the system used in the thesis). As pointed out in Section 2.324, it would be desirable to have a counter which would resolve and count 15 mc pulses, since this would decrease the conversion time without impairing the sensitivity of the system. At present, reliable counters that are effective above 5 mc are not available, but probably could be developed if a need arose. For the thesis work no counter was needed.

2.49 The Flip-Flops and Gate Tubes

The flip-flop and gate tube were described in Section 2.22. For the thesis two standard Whirlwind register panels[1] were used for the test setup to be described. A register panel contains a trigger tube (essentially a pulse amplifier), a flip-flop, and a gate tube. Two of these panels form the two flip-flop and gate tube combinations of a test setup to be described. One extra gate tube is needed, and it is obtained from a gate tube panel,[2] which is a standard Whirlwind panel containing three gate tubes and associated circuits.

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1. Ref. 21
2. Ref. 22

If the clock pulse frequency is to be higher than 4 mc, flip-flops and gate tubes would have to be used which could operate fast enough so that the rise and fall times of the gates would be small compared to the interval between two clock pulses. The rise time of the gates in the equipment used is less than 0.2 microseconds, and the fall time just about 0.2 microseconds.

The oscilloscope used for test purposes was a DuMont type 256B.

2.5 TEST PROCEDURES AND RESULTS

In this section we will discuss the actual operation of the system, the adjustments that must be made, and the results obtained.

2.51 Test Setup

Since the stator frequency is 4 kc in the system used in the thesis, a control pulse will occur once every 250 microseconds, followed by a code pulse (on a separate line). A system (shown in Figure 14) was set up so that we could sample the information contained in the pairs of pulses at any desired rate up to about 100 times per second. It is desirable to sample the information at low rates for two reasons: (1) it more nearly simulates the conditions the system would meet when used in conjunction with the computer, where the shaft position would be sampled about once every 1/50 second, and (2) to use this setup in conjunction with the decoder being developed as the other part of the thesis, it is necessary to feed information to that system at relatively low rates.

The test setup shown in Figure 14 works as follows: The blocking oscillator will produce pulses at a variable repetition rate of from zero

(push button) to over 100 pulses per second. (See Figure 36.) Let us see what happens following the arrival of one of these pulses at flip-flop 1 (FF 1).

Both flip-flops are initially in the cleared position (set to 0) so that all gates are closed. The pulse from the blocking oscillator sets FF 1 to 1, opening its gate tube. The next control pulse to come along will pass through this open gate tube and go on to the output equipment. This control pulse will also set FF 2 to its 1 position and therefore open both of its gate tubes. Clock pulses will pass through the lower gate as long as it is open. These pulses are used for test purposes as will be described shortly. The next information pulse to arrive after the control pulse will pass through the upper gate tube connected to the second flip-flop and go on to the decoding setup. It will also shut off FF 2 (i.e., set it to 0).

This system thus allows a single pair of pulses carrying information about the shaft position to pass through it only at the command of the pulses from the blocking oscillator (or some other asynchronous source of command pulses). It is similar to systems that might be used in computers which would send pulses to a counter only when reading a shaft position, leaving the counter free for other uses at other times.

The lower gate tube attached to FF 2 is very convenient for test purposes. Note that FF 2 turns on at the command of the control pulse and off at the command of the information pulse and therefore can serve as the flip-flop shown in Figure 2 which is used to gate the pulses going to the

counter. The extra gate tube is used for this purpose and gates the 4 mc pulses coming from the clock; it serves as the gate tube shown in Figure 2.

In the results described below, the number for a given position of the shaft was obtained by actually counting on an oscilloscope the number of clock pulses passing through this gate tube. The oscilloscope was synchronized with the control pulses and the cathode ray tube had sufficient persistence so that even when the information was being sampled at push-button rates the pulses could be seen and counted. Marker pulses occurring every ten and every one hundred clock pulses were also presented on the oscilloscope to facilitate counting. These pulses were derived from the 1000 to 1 divider chain. Figure 14a shows 10 pulses which would set a counter to the binary number 1010. The marker pulses are also shown. This method of counting pulses eliminated the need for setting up a 10-stage binary counter.

Figure 22 is a picture of the test setup.

2.52 Quantitative Results

2.521 Sensitivity

It was shown in Section 2.325 that the parameters used in this thesis should give a sensitivity of 1/1000, and it is found that this is the result. Figure 16 shows the position of the shaft for ten successive numbers of pulses. Note that a change in the shaft position of about 0.36 degree will increase the number of pulses by one. Observing the count on the oscilloscope for a given position of the shaft showed that there was very little jitter, and that there was no tendency for the number of pulses to change (as long as the shaft was held fixed) even over periods of several hours.

2.522 Accuracy

As was expected, the accuracy of the system is not equal to the sensitivity. It is within the limits set at the outset, namely the binary pulse-coded number will represent the actual position of the shaft to within 1.0 degree, (i.e., the accuracy is 1/360 as defined in Section 2.323). Figure 17 shows the type of error curve obtained after a typical adjustment of the system. The angle of the shaft for every increase of 50 pulses was measured and compared with the angle calculated from the number of pulses by means of the linear relation

$$\theta = \frac{\text{no. of pulses}}{1000} \times 360 = \text{shaft position in degrees.}$$

In Figure 17, the error is plotted as a function of the number of pulses. Note that at no time does the error exceed 1.0 degree.

2.523 Adjustment of the Phase-Shifting Networks

The accuracy obtainable from this system is directly dependent upon the phase adjustments in the networks which perform the single-to-three-phase conversion. The method of adjustment requires some consideration.

The only simple method of adjusting these networks quickly and simply that we could develop is the so-called spinning rotor method.[1] In this method the rotor of the control-transformer is continuously rotated at several rps (a small motor was used for this purpose). It can then be shown that when the three phases are balanced, the output of the rotor will be constant in amplitude, but if there is any unbalance in either amplitude or phase, the rotor voltage will vary in amplitude as the shaft

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1. Ref. 5., p. 495

rotates. Thus the procedure is: With the rotor revolving, the rotor output is observed on an oscilloscope which is synchronized with the reference sinusoid. If there is an unbalanced condition, the result will be that shown in Figure 18b, but when the three phases are balanced, the amplitude will be very nearly constant as in Figure 18a.

The principle of this method can be explained by means of symmetrical components.[1] It is known that any set of three-phase voltages can be separated into three balanced components: the zero, positive and negative sequence components. If E_{na}, E_{nb}, and E_{nc} are the three line-to-neutral voltages applied to the stator, then the symmetrical components would be balanced three-phase voltages with amplitudes given by:

$$E_0 = 1/3\ (E_{na} + E_{nb} + E_{nc})\ ;\ \text{zero sequence} \qquad (1)$$

$$E_p = 1/3\ (E_{na} + E_{nb} \angle 120^\circ + E_{nc} \angle -120^\circ)\ ;\ \text{positive sequence} \qquad (2)$$

$$E_n = 1/3\ (E_{na} + E_{nb} \angle -120^\circ + E_{nc} \angle +120^\circ)\ ;\ \text{negative sequence} \qquad (3)$$

Assume for the purposes of this analysis that the rotor is open so that there is no armature reaction. It is assumed that the windings are sinusoidally distributed, have equal impedances, and are placed 120 degrees apart (mechanically). The magnetic flux in the air gap will be proportional to the currents in the stator windings, and, since the windings are all identical, proportional to the voltages applied to the stator. According to these assumptions, the rotating flux field in the air gap would have

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1. Ref. 23., Chap. XI., especially Section 5

the usual form $F = F_m \sin(\theta - \omega t)$, if the three-phase voltages are balanced. If they are not balanced, however, there will be a positive-sequence flux field (F_p) which is identical to F except in amplitude, and a negative sequence of the form $F_n = F_{nm} \sin(\theta + \omega t)$ where F_{nm} is proportional to E_n in Equation (3) above. E_n is small for a small unbalance and zero for perfect balance. The field due to the negative sequence rotates in the opposite direction from that due to the positive sequence (but at the same speed), and therefore causes the amplitude of the flux to vary as a function of the mechanical angle. That is, the negative sequence flux adds to the positive sequence flux in one part of the cycle and subtracts from it at another. The negative sequence flux field adds vectorially to the positive sequence flux and so prevents the phase shift of the rotor signal from being a linear function of the shaft position. Thus when using the spinning rotor method, any variation in the amplitude of the rotor signal as a function of θ will mean the three-phase voltages are unbalanced, and therefore the phase shift of the rotor sinusoid will not be a linear function of the shaft position. It might be noted that it is possible that the spinning rotor will give an indication of balance (no variation in amplitude) although there is a considerable unbalance which by coincidence happens to make the negative sequence go to zero. This, however, could only occur with unequal amplitudes among the three voltages, and it is easy to measure the three amplitudes to insure that they are equal.

In the actual tests it was found that another factor must be considered in the adjustment of the phases, and that is the harmonic content of the sinusoids applied to the stator. It can be shown that the second

harmonic of a three-phase signal applied to a device with three windings equally spaced about the core will produce a flux field which will rotate in the opposite direction from that produced by the fundamental harmonic, and at twice the frequency. This field will prevent the phase shift from being a linear function of θ and will cause the voltage amplitude of the rotor output to vary as a function of the shaft position, just as does the negative sequence component due to unbalance. The effect of harmonics will therefore mask the effects of the negative sequence flux field caused by an unbalanced condition when using the spinning rotor method. Although every attempt was made to get the harmonic content of the stator voltages as low as possible by means of filters, there was still enough second harmonic content so that it was not possible to use the spinning rotor method to balance the phases without placing a filter in the rotor circuits. Another low-pass filter placed in the rotor output (as shown in Figure 7) apparently eliminated the effects of the harmonics so that the spinning rotor method could be used. Of course, the rotor filter is needed not only so that we could use the spinning rotor method, but also so that the harmonics would not affect the linear relation between the phase of the rotor position and the shaft position. As Figure 16a shows, it was possible to get the amplitude of the rotor voltage practically constant as a function of shaft position.

In performing the accuracy tests the procedure was to (1) make sure that the amplitudes of the three stator voltages were equal, and (2) to adjust R_1 and R_2 in Figure 7 while spinning the rotor until the rotor output was constant. Since this procedure results in errors less

than 1.0 degree, it was felt that this method of adjustment was satisfactory both from the point of view of simplicity and from the point of view of the results obtained.

2.524 Nature of the Errors

The curves of error as a function of count (Figure 17) have a rather definite shape, and some attempts were made to correlate this error with the presence of either harmonics in the stator voltages of an unbalanced condition in those voltages. However, there seems to be no simple correlation with either of these factors. Actually, the exact shape of this error curve is masked by three additional factors:

(1) The output is quantized to the nearest 0.36 degree.

(2) The error in reading the protractor which indicated shaft position was probably about $\pm$ 0.15 degree.

(3) The synchro itself may have errors of the order of $\pm$ 0.15 degree.

In other words, in getting errors of less than 1.0 degree we are probably entering the region where experimental inaccuracies are accounting for a large part of the error.

Since no correlation between errors and possible sources seemed obvious, and because the error is less than the maximum considered allowable, no further attempt was made to find the sources of the error, or to try to eliminate them.

2.525 Stability

In this section we are interested in whether the system will operate satisfactorily despite variations in voltages, temperature, time,

aging of tubes and so on. In general there are two types of instability in a system of this nature; jitter, which means that the binary number for a given angle varies during a short period of time, and drift, which means that the number will change only after a long period of time (of the order of hours). It was found that the system was practically free of either type of difficulty.

To check for jitter, the shaft was set at some angle and information was read through the test setup (Section 2.51) at push-button rates to an oscilloscope. Each time the push button was operated, the number of pulses could be observed. In this way any jitter would show up. It was found that for a given shaft position the number of pulses remained constant each time the information was read. There is one case where some jitter was noticed, and that was if the shaft was set at such a position that a clock pulse was going to the counter just as the gate was turning off. The amplitude of this last pulse would vary, which would mean the number to which a counter was set might vary by one. This type of jitter is to be expected unless the rise and fall times of the flip-flop gates is considerably improved. Anyway, this would introduce an uncertainty of only 0.36 degree which is within limits of accuracy of the system. Other than this, the jitter problem did not exist.

In order to check for drift two different tests were made. First, an accuracy run was made on one day immediately after the system had been adjusted. Then, three days later, after the setup had run about 16 hours, and had been shut down twice and turned on again, another accuracy run was made without adjusting anything. It was found that the zero number

was still zero angle, and the accuracy was still better than 1.0 degrees. Compare curves in Figure 17.

It was noticed that during the first one-half hour after the equipment is turned on that the number of pulses for a given shaft position would change by as many as 5. This was principally due to a change in the zero position. Since the equipment settles down and is very stable after the first one-half hour, this warm-up drift is not considered serious.

The second type of drift test was simply to set the shaft at a known position and measure the number of pulses. After some hours the number of pulses is measured again to see if there has been any change. This test has been repeated several times, each time running for 2 to 5 hours, and during none of these tests did the count change by more than one (equivalent to 0.36 degree) always excluding the warm-up period.

A series of tests were made in which the change in number of pulses was measured as a function of various voltages while the shaft was held fixed. The following voltages in the clipper-peaker were varied $\pm$ 5%: peaker plate voltage, peaker bias voltage, screen voltages of each of the clipper stages, and the voltage amplitude of the gate from the gate generator (by varying the input potentiometer in Figure 7). In no case did the number of pulses in the output change by more than one. In general if the voltages are held to $\pm$ 5% no trouble with drift is expected. Aging of tubes, which is simulated by lower screen voltages, should not cause any trouble either.

One other test was made in which the frequency of the clock was varied, and the number of pulses measured for a given shaft position.

As is to be expected, since the stator frequency is synchronized with the clock frequency, the number of pulses per degree remains the same over wide ranges of frequency. That is, the relative accuracy remains high. The frequency was varied by $\pm$ 2% with no change in relative accuracy. There was, however, a change in the actual binary-number output for a given shaft position which was due to a change in the zero position. It appears that some of the components in the system have a phase shift which is dependent on frequency, and this, as we have seen (Section 2.3232) will cause a change in the zero position. Even this change was small, however, being such that a 1/4% change in frequency is needed to give a change in the binary number of one out of 1000. This stability is probably sufficient in most cases, since even non-crystal controlled oscillators can be made stable to better than $\pm$ 1/4%. If, however, better stability is required, then this change in zero position with frequency could probably be eliminated by redesign of the rotor filter network or other components which may also give trouble of this nature. At any rate, this order of stability is considered sufficient for most purposes.

2.526 Tests Using Two Control Transformers

In order to show that this system will work properly when the position of more than one shaft is to be measured, the following test was made: Two control transformers were operated with their stators in parallel. (The change in impedance levels due to the added load had no effect on the circuits.) The balancing adjustments were made by using the spinning rotor method on the second control-transformer, and then an accuracy test was made using the first one. The results are shown in Figure 19. Note that

the accuracy was always better than 1.0 degree. This test proves that at least two control transformers can be operated with their stators in parallel without requiring separate balancing adjustments for each one. Although this was only a two-unit test, there is no evidence that the system cannot be extended to a large number of units if provision is made to supply the required power to drive that low impedance load.

One other change was made before this two-unit test was performed. We noted in Section 2.441 that placing a filter network directly in the rotor output tended to affect the stator waveforms due to interaction through the armature flux field. This distortion would prevent operating two units in parallel since the distortion from one unit would affect the readings given by the other one in random fashion. In order to eliminate this effect a cathode follower was built (see Figure 20) which acted as a buffer between the rotor and the filter network. Since the input impedance of the cathode follower is high, no appreciable armature current was drawn, and the stator voltages were unaffected. (The small loss in gain through the cathode follower stage is unimportant.)

Note in Figure 20 also that the filter used after the cathode follower is slightly different than that used previously in the rotor circuit (see Figure 7). This filter seemed to give better results, probably because it eliminates second harmonics more effectively.

The exact procedure used in this two-unit test was to put the cathode follower on the second control-transformer rotor, observe the c.f. output on an oscilloscope, and adjust the phases by use of the spinning

rotor method. The cathode follower was then shifted to the other control-transformer with the output of the cathode follower going to the second clipper-peaker as usual. An accuracy check was then made.

2.53 Summary of the Results

The system developed in this thesis for converting shaft positions into binary pulse-coded numbers has the following characteristics:

Sensitivity: 1/1000 of a revolution of the shaft.

Accuracy: 1/360 of a revolution.

Time required to convert the largest number: 250 microseconds

Reliability: excellent. Adjustments should not need attention oftener than once a week.

Although the system is not ready for any specific use, it can be adapted to the needs of any system with very little further research.

2.6 SUGGESTIONS FOR FURTHER RESEARCH

2.61 The Resolver Phase-Shifting Method[1]

We have seen that one of the difficulties in the system of converting between shaft position and binary pulse-coded number described above is in adjusting the phase-shifting network so that the three phases are properly balanced. There is an alternate method which may be used in which the problem of generating and balancing three-phase voltages does not arise. This system will be described although no work was done on it as part of this thesis.

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1. Ref. 5., p. 498

If a synchro resolver (which is similar to the control-transformer but with a two-phase stator) is connected as indicated in Figure 21, it can be shown that the output will be

$$E_{out} = K \sin (\omega t + \theta + 45^{\circ})$$

if R and C are chosen so that $R\omega C = 1$. (K is a constant, θ is the angular shaft position.) Thus the phase of the output shifts as the shaft rotates even though there is no rotating flux field in the resolver. By using this system no three-phase voltages are required anywhere.

The advantages of this resolver system could be:

(1) simplified adjustment procedure.

(2) stability of adjustments over a long period of time.

The disadvantages of this system might be:

(1) An adjustment (to make $R\omega = 1$) is required for each shaft to be measured.

(2) No filter or phase-shifting adjustments can be placed directly in the output from the resolver. This means a buffer stage would be required, but we have seen that this may be true in any case.

This resolver system should be tested and compared with the system using the control-transformer before a choice between the two methods is made.

2.62 Changes in the Clipper-Peaker Circuit

There are several modifications that might be made in the clipper-peaker circuit, which would simplify the system.

2.621 Input Stages

We have mentioned that placing a filter directly in the output of the rotor (of the control-transformer) may have two detrimental effects:

(1) It will introduce an unwanted phase-shift if the stator frequency changes, resulting in a shift in the zero position.

(2) It acts as a load on the rotor which then draws current. The rotor current reacts on the stator voltages (through the armature flux field), and this effect may prevent the paralleling of control-transformers.

In Section 2.526 we showed that a cathode follower between the rotor and the filter would eliminate the second of these effects. There is no reason, however, why this buffer stage could not be a linear amplifier stage, which would still have the high impedance input, but would also amplify the rotor signal. This amplification would (1) improve the effectiveness of the clipping stages that follow, and (2) allow one to use a better filter between this amplifier stage and the clipper-peaker since any loss in the filter would be compensated by this added amplification. Also, because of the isolation provided by the extra stage, the filtering could be more easily adjusted so that it did not introduce any phase shift as a function of frequency.

This additional stage could probably be added without increasing the number of tube envelopes required in a rotor output channel by making the first tube of the clipper-peaker a dual triode (e.g., 2051). The first triode stage would be the buffer and would amplify the rotor simusoid linearly. This stage would be followed by a filter similar to that used in the cathode follower circuit (Figure 20), or a better filter if needed. Then the signals would be clipped and amplified, (as they now are in the first clipper-peaker stage), using the other triode in the envelope for

this purpose. The other clipper stage and the peaker would remain the same.

2.622 The Overshoot Problem

It is suggested that more work be done on the problem of eliminating the overshoot in the output of the second clipper stage (V_2 of Figure 9). The crystal diodes used to eliminate the effects of overshoot are effective but have the disadvantage of lowering the gain of the stage. An increase in gain would increase reliability (although no evidence was found of unreliable operation).

2.623 The Peaker Stage

The peaker stage is entirely satisfactory, but it should be pointed out that because of the long deionization times required by gas tubes, this type of peaker would not work well if the stator period (t_s) is much shorter than 100 microseconds. For shorter periods than this either a vacuum tube or a crystal-gated RLC peaker[1] followed by a buffer amplifier would have to be used.

2.63 Higher Accuracy Systems

Even if the effects of harmonics and unbalance are eliminated, it is not likely that the accuracy obtained by use of a single control transformer per shaft can be made greater than 1 part in 500. As we have mentioned before, it is necessary to use two-speed systems[2] to obtain higher accuracy. For example, a shaft could be geared to the control-transformer by a 100 to 1 ratio, so that the over-all accuracy would become 1 part in

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1. Ref. 7., p. 2-72
2. Ref. 5., p. 443 and Ref. 2., pp. 19-22

3.0 CONVERSION OF BINARY PULSE-CODED NUMBERS INTO VOLTAGE AMPLITUDES

3.1 REQUIREMENTS TO BE MET

In the Introduction, it has been shown that when a digital computer is to be used as part of an information-processing system, devices are required at the output of the computer which convert binary pulse-coded numbers into analog quantities. These devices are called decoders. In particular, we will here consider decoders which convert binary numbers into voltage amplitudes, since voltage amplitudes are frequently used as commands for a controlled system.

One of the reasons why digital computers are well suited for use in an information-processing system is that they can be made to have high accuracy, providing sufficiently great number length is used. But the accuracy of the computer is effectively lost if it is coupled to the rest of the system by conversion devices of low accuracy. While digital computers can be made to have an accuracy of 1 part in 10,000, it is very difficult to obtain that same accuracy in a single decoder, and frequently such stringent demands do not have to be met. Considerable improvements in the performance characteristics of a given decoder can be realized by the use of a feedback system (a decoder of moderate accuracy in the feed-forward section and a coder of high accuracy in the feedback section), but it is nevertheless required that a decoder have an accuracy better than 1 part in 100.

In a complex information-processing system, there will be many channels which are to receive information from the computer. It would be

uneconomical to equip each channel with a complete decoder. The design of the decoders must therefore be such that they may be shared, at least partly, by as many of the controlled channels as possible. The decoder can then be switched temporarily into that channel which is to receive the instantaneous output of the computer. The switching process is highly practical, since the computer can furnish information to only one channel at a time. For this reason, the computer will supply information to any one channel in the system not continuously, but at irregular intervals. It is therefore required that a decoder maintain the given information until new information is furnished. This requirement makes it clear that only a part of a decoder can be shared by several channels in the system; some other part of the decoder must be unique to a single information channel, so that a given channel may retain the previous input while the others are supplied new information. The "holding" requirement is further complicated by the fact that the computer will furnish information at irregular intervals, the length of the intervals being determined by the complexity of the calculations which the computer is carrying out. Before new information is furnished to any given channel, that channel must be prepared to accept it. This preparation could be done by sending to the decoder a preliminary signal shortly before the new information is supplied. But such a procedure puts an additional burden on the programming of the computer and should be avoided. Instead, the decoder must be able to accept information at any time.

Since one of the main purposes in employing a modern computer in an information-processing system is the attainment of high speeds of

operation, it is surely required that the associated decoders as well as the computer operate rapidly. But, because there are a number of channels which are to be controlled by the computer and, consequently, each channel receives information at a rate smaller than the operating speed of the computer, it is, in general, not required that the decoding process be carried out in the interval between successive solutions obtained by the computer. Rather, the maximum decoding time is limited by the minimum time interval between successive pieces of information supplied to a given channel, if the resulting time lag can be tolerated by the rest of the controlled system. Thus system as well as computer characteristics enter into the determination of the maximum permissible decoding time. However, the characteristics of the decoder must be such that it can accept information from the computer in less time than is required by the computer to arrive at two successive results. If this were not true, the operation of the computer would be slowed down by the decoding process. The speed requirements placed on decoders are then as follows:

(1) The decoder must accept information very rapidly. This requirement is governed by the operating speed of the computer.

(2) That part of the decoder which is to be shared by several channels should operate at the highest possible speed, so that its use may be shared by the maximum number of channels.

(3) That part of the decoder which is unique to a single channel need not necessarily operate at a speed greater than the rate at which information is supplied to that channel.

Reliability and stability requirements are affected by the obvious demand that the calibration of the decoder be constant over the longest

possible periods of time. The potential reliability of a decoder can be gauged by the number of vacuum tubes used in the design, since vacuum tubes are the largest single source of failures in electronic circuits. Reliability is thus intimately connected with simplicity of design.

Practical considerations demand that the decoder be insensitive to small variations in supply voltages. In view of the accuracy demands, this requirement is hard to fulfill. It may well be that the characteristics of the decoder demand good regulation of some of the supply voltages, but the number of closely regulated sources should be kept to a minimum.

3.2 HISTORY OF THE PROBLEM*

3.21 The Shannon-Rack Decoder

The need for conversion of binary numbers to voltage amplitudes is not unique to the application of digital computers to information-processing systems, but is also encountered in pulse-code modulation, where samples of the transmitted signal appear at the receiver in the form of binary-coded pulse groups. Thus the process of demodulation in pulse-code modulation is one of converting binary-coded pulse groups, which may be considered to represent binary numbers, into voltage amplitudes.

Workers in the field of pulse-code modulation have developed several schemes for decoding. W. M. Goodall[1], C. E. Shannon[2], A. J. Rack[2], and A. H. Reeves[3] have designed systems to perform the conversion of binary numbers to voltage amplitudes. Most promising among these is the decoder

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* For a more complete description of previous work in the field, see Ref. 4.

1. Ref. 25
2. Ref. 26
3. Ref. 27

suggested by Dr. Shannon and modified by A. J. Rack. In the operation of this decoder, pulses representing the binary number arrive at the input to the decoder serially in time, spaced apart by an amount t_o. Each pulse turns on a constant-current source for a fixed time interval and thereby deposits an equal amount of charge Q on a condenser, which, in parallel with a resistor, is connected to the constant-current source. The time constant of the R-C circuit is so arranged that during each time interval t_o the charge on the condenser, and hence the voltage across it, decay to one half of the original value. Assume that the number to be decoded contains no more than five binary digits. The digit 1 is represented by the presence of a pulse and the digit 0 by the absence of a pulse. The 2^0-digit pulse arrives first, the 2^1-digit pulse second, etc. At the end of five intervals t_o, the first pulse in the train will have contributed Q/32 units of charge to the condenser, the second Q/16, the third Q/8, the fourth Q/4, and the fifth Q/2. Since the system is linear, the contributions of the individual pulses add, so that the voltage on the condenser at the end of the fifth interval is directly proportional to the number to be decoded.

This is certainly a simple and effective way of decoding and has been successfully employed in the Bell Telephone Laboratories' pulse-code modulation system. But the Shannon-Rack decoder does not contain any feature for maintaining the output constant during the interval between decoding operations. While storage of the output voltage of the decoder can be accomplished by an additional condenser, this method of storage is not satisfactory in applications where the time interval between successive

decoding operations may be long. The accuracy of the Shannon-Rack decoder is quite good (accuracy of 1 part in 128 has been accomplished), but it cannot be extended indefinitely since it is limited by the uniformity with which charges can be deposited on the condenser in the R-C network.

The Shannon-Rack decoder can be shared by several channels only by switching its final output to the desired channel. Switching of voltage amplitudes without loss of accuracy is a difficult task, and the need for it represents a disadvantage of the decoder. Finally, it should be noted that the operation of the Shannon-Rack decoder demands that the pulses of the binary number to be decoded arrive serially in time. For this reason, the device cannot be used directly in those applications where parallel transmission of digits (i.e., the transmission of all digits simultaneously over a set of separate lines, one for each digit) must be carried out.

3.22 Binary-Weighted Decoders

Other decoders have been developed which contain the "holding" feature. Prominent among these is a unit developed by J. O. Ely for Project Whirlwind.[1]

This decoder operates on the following principle. Each pulse representing a binary digit causes constant-current sources weighted in accordance with the value of the digit to send current through a common load resistor. Thus the 2^0-digit pulse causes 1 unit of current to flow through the load resistor, the 2^1-digit pulse causes 2 units of current

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1. Refs. 28 and 29

to flow through the load resistor, etc. The voltage across the common load resistor is proportional to the number to be decoded.

The disadvantage of Ely's decoder lies in the fact that a complete decoder has to be provided for each output channel. Since each unit requires a considerable number of tubes, this particular decoder, although accurate and reliable, is not suited for an application where many elements in the system share the output of the computer. (The design of this decoder was not intended for use at the output of the computer, but rather as a deflection-voltage generator for the electrostatic storage tubes which the Whirlwind computer uses.)

3.23 Sard's Decoder

A decoder which allows sharing of part of the unit by several channels has been developed by E. W. Sard.[1] According to this design, decoding proceeds in three steps: First, the binary number is converted into a pair of pulses, the time interval between which is proportional to the binary number to be decoded. Second, the first and second pulse of this pair determine the beginning and end, respectively, of a rectangular voltage waveform. Third, this waveform is linearly integrated. The output of the integrator is directly proportional to the binary number to be decoded. Because the method of decoding developed by Sard is basic to the operation of the decoder described in this thesis, the operation of Sard's decoder will be discussed in some detail.

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1. Ref. 30

The first step of the decoding process is performed by a binary counter. While the binary counter actually used by Sard is somewhat different from the one shown in Figure 1, that figure can still be used to explain the principle by which a binary number can be converted into a pair of pulses, the time interval between which is proportional to the binary number to be decoded. Consider Figure 1 and assume that the counter has only four stages, as shown. With the counter originally cleared, it will then take 16 pulses at the input line in order to get an output pulse from GT4. If, however, the counter is not initially cleared before pulses are admitted to the input line, the number of input pulses required to obtain an output from GT4 will be less than 16. In general, the number of pulses necessary to obtain an output pulse from GT4 is 16 diminished by the number to which the counter has been preset.

The first pulse of the desired pair is the initial pulse applied to the input of the counter, and the second pulse is the output of GT4, providing the counter has been preset in such a manner that the output pulse of the counter occurs at the proper instant, i.e., the time interval between the initial pulse and the output pulse is directly proportional to the number to be decoded.

How shall the counter be preset? Since the input pulses to the counter are of fixed repetition rate, there is a direct proportionality between the number of pulses required to obtain an output from the counter and the time interval between initiation of counting and the appearance of the output pulse from GT4. The counter must therefore be preset in such a manner that the number of pulses required to obtain an output pulse

will be equal to the number to be decoded. The correct relationship between the number to be decoded and the number to which the counter is to be preset is

16 - (number for presetting) = number to be decoded

or, number for presetting = 16 - number to be decoded,

which is in binary notation

number for presetting = 10000 - number to be decoded

or, number for presetting = 1 + (1111 - number to be decoded) (3.1)

The number in parenthesis is the nines complement of the number to be decoded.* Since in the binary system the nines complement of a number is found by replacing every 1 by a 0 and every 0 by a 1, it is very easy to find the nines complement by electronic means. One merely puts pulses in those digit columns where there are none, and removes pulses from those digit columns which have them. For this reason, it is convenient to preset the counter to the nines complement of the number to be decoded, although Eq. 3.1 does not apply strictly. For the case when the counter is preset to the nines complement of the number to be decoded, it will take one more input pulse than the number to be decoded in order to obtain an output pulse from the counter.

The procedure for carrying out the first step of the conversion is thus clear. A binary counter, preset to the nines complement of the number to be decoded, is supplied constant-frequency pulses. The first

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* The nines complement of a number is that number which when added to the given number yields a "nine" in all digit columns, where nine is interpreted as the greatest digit possible in the number base used. In the binary system, 1 is the greatest possible digit.

pulse admitted is the first pulse of the desired pair, and the output of the counter, commonly called the counter end-carry, is the second pulse of the desired pair.

The second step of the decoding process is very simple. The first pulse admitted to the counter is used to trigger the leading edge of the rectangular waveform, and the counter end-carry is used to trigger the trailing edge of the rectangular waveform.

The final step of the conversion consists of linear integration of the rectangular waveform, so that the output of the integrator will be directly proportional to the binary number to be decoded. Truly linear integration is required, and while this is by itself a stringent demand, the operation of the integrator is even more complicated by the demand that the integrator hold the output until a new number is to be decoded.

This last step proved to be the weak part of Sard's decoder and measurements indicated that the accuracy of the decoder was only $\pm$ 2%. Clearly, an alternative way for converting a pair of pulses, the time interval between which is proportional to the binary number to be decoded, has to be found, if the advantage of time-sharing, inherent in a decoder of the counting type, is to be realized. In this thesis, such a method is described.

3.3 THE DECODER INVESTIGATED IN THIS THESIS

3.31 The Complete System

The complete decoder proposed in this thesis, shown in the block diagram of Figure 23, is an extension of previous work on decoders of the counting type. It may be considered to consist of two parts, a binary counter[1]

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1. Ref. 24

and the so-called conversion device, which will be described in detail in the following sections. The purpose of the counter is to convert the binary number to be decoded into a pair of pulses, the time interval between which is proportional to the number to be decoded. The manner in which this can be done has been discussed in the previous section. It is the function of the conversion device to change the pair of pulses which arrives at its input to a voltage amplitude which is directly proportional to the binary number to be decoded. The entire decoding process thus consists of two steps: the conversion of a binary number into a pulse-position-modulated signal and the conversion of a pulse-position-modulated signal into a voltage amplitude.

In the operation of the system, the computer furnishes, in addition to the nines complement of the number to be decoded and a control pulse which starts the counting action, control pulses to the switch. Since the output of the computer is to be shared by many channels, the computer must furnish signals which will, at the desired instant, cause the proper channel to receive the information from the computer. This selection of channels is here carried out by the switch, which is set in accordance with the control signals coming into the switch on the line shown at the lower left of Figure 23. The switch connects the selected channel to both the counter-end-carry line and the start-count line.

A complete decoding operation will then consist of the following series of steps:

(1) The computer sets the switch, thereby connecting one of the n channels to the counter-end-carry and start-count lines.

(2) The computer presets the binary counter to the nines complement of the number to be decoded.

(3) The computer sends out the start-count pulse, thereby

(a) sending one pulse to the selected channel

(b) initiating the counting action.

(4) Upon the arrival of the start-count pulse, pulses from the fixed-frequency pulse generator are admitted to the binary counter.

(5) After a number of pulses equal to 1 + the binary number to be decoded have been received from the pulse generator, a counter-end-carry pulse appears at the output of the counter. We will call the counter-end-carry pulse the INFORMATION PULSE, since its position in time, with respect to the start-count pulse, is directly related to the binary number to be decoded. We will call the start-count pulse the CONTROL PULSE.

(6) The information pulse enters the conversion device in the selected channel.

(7) The selected conversion device produces an output voltage which is proportional to the binary number to be decoded. The decoding process is now completed.

It is noted in Figure 23 that only one binary counter is needed and that its output, the information pulse, is shared by the n channels. Therefore, the binary counter is that part of the decoder which is made common to several channels. The decoder here described thus meets the

requirement that part of the unit is to be shared by several of the output channels. The number of channels which can be connected to the same counter depends upon the interval between successive readings to a single channel. The more frequently information is to be furnished to a single channel, the smaller will be the total number of channels which can be connected to the counter.

Without considering a particular application, one cannot say what the interval between successive readings to a single channel will be. However, in order to give some indication of possible conditions, we will here arbitrarily assume that each channel is to receive information 50 times per second, and on that basis establish the number of channels to which a single binary counter may be connected.

A binary counter employing the basic electronic circuits used in the Whirlwind computer can be operated at a pulse repetition rate of several million per second. A conservative figure and one which results in unquestionably reliable operation is two million per second. If it is desired to convert an eight-digit binary number into the corresponding pair of pulses, it will then require, in case of the maximum possible number (255),

$$(255 \times \tfrac{1}{2}) + \tfrac{1}{2} = 128 \text{ microseconds}$$

to obtain the desired pair of pulses. (See Eq. 3.1.) If 50 such conversions per second are to be made for each channel, then each channel will be connected to the counter for

$$50 \times 128 = 6400 \text{ microseconds}$$

out of each second. Thus we see that under the given conditions, and making

allowance for the time required to clear the switch and other control operations, approximately 150 channels may be connected to the same counter.

This is a very high figure, and perhaps greater than would be encountered in any practical case. If there really were 150 different output channels and each had to be furnished information 50 times per second, the computer would have to arrive at 7,500 solutions per second, a figure larger than is presently anticipated. However, the above example does serve to point out that in a controlled system the proposed method of decoding is thoroughly practical, since the need for only one binary counter exists. Indeed, its use may probably be shared by all the input channels as well as all the output channels.

The decoding system described here demands that the switch connect the control pulse and the information pulse to the selected channel. This is an easy task to accomplish, since the switch is called upon to handle only pulses of fixed amplitude. A crystal-matrix switch of the type used in the Whirlwind computer is very well suited for this application and can be expected to give fully satisfactory performance.[1] It should be noted that the need for a switch does not introduce any additional equipment, since any system would require that the output of the computer be distributed in some manner to the various output channels. The manner of distribution here chosen (in which only pulses are switched) is the most favorable one known.

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1. Refs. 20, 31, and 32

It has already been mentioned that the binary counter and the crystal-matrix switch required in this method of decoding are well known and have been designed and constructed as parts of the Whirlwind computer. No purpose would therefore be served in incorporating their design in this thesis investigation. The investigation has therefore been restricted to the design, construction, and testing of the so-called conversion device, i.e., the part of the decoder which converts pairs of pulses into the corresponding voltage amplitudes. The following sections will describe a novel conversion device, its design, and its characteristics.

3.32 The Conversion Device

3.321 Functional Description

In the discussion of desired characteristics of decoders to be used in an information-processing system, it has been shown that a decoder is required to maintain the given information in the interval between successive readings to the particular channel in which the decoder is located. In the method of decoding proposed in this thesis, the "holding" action must therefore be incorporated in the so-called conversion device, since the binary counter must be free to operate in conjunction with all of the n conversion devices. The function of the conversion device is thus twofold: conversion of a pair of pulses into a voltage amplitude, and "holding" of that amplitude for periods of time perhaps as long as one second.

The "holding" action is the harder one to accomplish. It is particularly troublesome when the actual amplitude of the desired voltage is set up only for a short instant and then impressed on a storage device such as a condenser. Condenser leakage causes a drop in stored charge,

thus introducing errors. If it is desired to change the stored charge after a new decoding process, the removal of the previously stored charge is a time-consuming process. One may think of this method of "holding" of information as storage in the voltage domain.

In order to avoid difficulties such as the ones mentioned above, the conversion device described here does not attempt to keep the final output voltage constant by direct means, but rather by indirect ones. It may be considered to achieve the "holding" feature in the time domain. This appears to be a more suitable approach to the "holding" problem, since electronic circuits can accurately control and reliably maintain timing.

Previous discussion has shown that at the input of a conversion device there will be a single pair of pulses for each reading operation to that channel. "Holding" is here accomplished by regenerating this single pair of pulses indefinitely. How this is achieved is shown in the block diagram of the conversion device, Figure 24.

Disregard for the moment the clear lines and delay elements 1 and 2 (DE 1 and DE 2). The control pulse enters delay element 3, where it emerges a time interval T_1 later. It is then returned to the input of DE 3 and also triggers the gate generator. The gate generator is so arranged that an output from DE 3 causes the leading or positive-going edge of the gate output to be generated. Since the first output of DE 3 was also fed back to the input of DE 3, another pulse emerges at the output of DE 3 T_1 seconds later and will keep emerging from DE 3 after every T_1 seconds. The initial control pulse is thus being kept "circulating" in DE 3. Every time there is an output from DE 3, the gate generator is triggered.

Some time after the control pulse, an information pulse appears at the output of the binary counter. It enters delay element 4, where it emerges a time interval T_1 later. At that instant, it is immediately fed back to the input of DE 4, where it is kept "circulating" in the same manner in which the control pulse is kept "circulating" in DE 3. Whenever the pulse emerges from DE 4, it triggers the gate generator, causing the trailing or negative-going edge of the gate output to be generated. The delay T_1 must be greater than the longest possible time interval between the incoming control and information pulses.

There is only one pair of pulses fed from the counter to the conversion device, but we see at once how, through the action of DE 3 and DE 4, a series of pairs of pulses is generated and hence a series of gates the length of which is proportional to the binary number to be decoded. The holding action is thus accomplished, and it remains only for the integrating network to remove the average value of the series of gates generated in order to obtain a voltage amplitude which is proportional to the binary number to be decoded. (It should be kept in mind that the voltage amplitude of the gates is fixed, and only their length varies with the number to be decoded. Thus the average voltage of the waveform carries the information.)

The purpose of delay elements 1 and 2 and the "clear" lines will now be explained. It has been shown that both the control pulse and the information pulse are kept "circulating" in their respective delay elements indefinitely. Consequently, when a conversion device is supplied with a new pair of pulses from the switch, confusion between the old pulses and

the new ones would result, unless the old pulses are made to disappear. A pulse is therefore required which will clear DE 3 and DE 4. Since it is desired not to burden the computer with the demand that a separate clear pulse be supplied before the new binary number is read out from the computer, the control pulse is used to carry out the clearing operation. After DE 3 and DE 4 are cleared, there has to be a short time interval before new pulses are sent to DE 3 and DE 4. DE 1 and DE 2 provide this "waiting" period by delaying both the control pulse and the information pulse before they enter DE 3 and DE 4, respectively. For purposes of explanation, we will here assume that DE 1 and DE 2 are set for exactly equal delays, so that the time relationship between the control and information pulses is not destroyed. More will be said about setting DE 1 and DE 2 in Section 3.3224.

The complete operation of the conversion device can now be described on the basis of Figure 25. This figure shows the time relationship between pulses in the conversion device, following the arrival of a control pulse from the computer. The control pulse first clears DE 3 and DE 4, then enters DE 1 where it emerges T_0 seconds later. At time T_2 the information pulse arrives, and in order to maintain its time relationship with respect to the control pulse, the information pulse is also delayed a time interval T_0 before it enters DE 4. DE 3 and DE 4 are adjusted to furnish exactly equal delays T_1, where T_1 is greater than the longest possible interval between a control pulse and an information pulse. The "circulating" action of DE 3 and DE 4 results in the series of pulses at the output of DE 3 and DE 4, and hence in the series of gates formed at the output of the gate generator.

The success of this method of decoding depends on the accuracy with which the delays in DE 3 and DE 4 can be made equal. If these two delays are not exactly equal, then the time relationship between the "circulating" pulses will be distorted from that which existed between the original control and information pulses. The core of the problem is then the achievement of identical delays T_1 in DE 3 and DE 4, and the design of these units must be carried out with great care.

The method of attack for the design of DE 3 and DE 4 must, of course, be based on the length of the delays which these circuits are required to furnish. The required delays are dependent on the over-all specifications which the decoder has to meet. These, in turn, are determined by the particular application at hand. Since this thesis investigation was not intended to serve only a particular case, general requirements were drawn up, with the aim of making them sufficiently stringent to satisfy many of the actual situations which may be encountered.

First, it was decided that the decoder designed here shall decode binary numbers ranging in magnitude from 0 to 255. This determines at once the required accuracy as 1 part in 256.

In order to simulate conservative operation, it was decided that the counter shall operate at a pulse-repetition rate of 2 million per second. Previous discussion has shown that under these conditions of operation, the information pulse will arrive 128 microseconds after the control pulse when the maximum number (255) is to be decoded. It is then seen that DE 3 and DE 4 must furnish delays somewhat greater than 128 microseconds.

Accurate and stable delays can be achieved most readily by delay lines. However, these lines can furnish delays no longer than about 10 microseconds, while approximately 130 microseconds of delay are here required. One could achieve this long delay by a cascaded arrangement of delay lines interconnected by pulse-shaping and amplifying stages. But such an arrangement would require a prohibitively large number of vacuum tubes. The use of delay lines must therefore be ruled out as a possible method of attack for this design.

Another excellent way of obtaining delays is by the use of acoustic delay elements such as mercury delay lines. When properly controlled, they could fulfill the requirements of this design very well. But their high cost and the relative complexity of the necessary control equipment make their use undesirable in this investigation.

The only other method of obtaining the required delays by simple and well-known means is through the use of trigger circuits employing vacuum tubes. Here the inherent accuracy of the delays is not as high as in the previously mentioned components. The design problem consists of surmounting this difficulty and developing trigger circuits which are sufficiently accurate for use in DE 3 and DE 4.

Monostable multivibrators are here used as the basic parts of DE 3 and DE 4. It has been shown that, in order to obtain the "holding" feature in the time domain, the outputs of DE 3 and DE 4 must be fed back to their respective inputs. Since the output of a multivibrator cannot be used directly to trigger the same multivibrator, it becomes apparent that DE 3 and DE 4 cannot be made up of a single monostable multivibrator.

Instead, this design uses a cascaded arrangement of two multivibrators for each of these two delay elements. In each of these, the first multivibrator triggers the second and the second, in addition to triggering the gate generator, also triggers the first multivibrator. The block schematic of the conversion device, shown in Figure 26, is thus evolved, with multivibrators 1 and 2 making up DE 3 and multivibrators 3 and 4 making up DE 4.

It has already been shown that the time delays in DE 3 and DE 4 must be exactly equal. This demand cannot be met by simple monostable multivibrators, since there is known to be some jitter, i.e., variations in the length of time during which the normally-on tube is cut off, in the operation of these circuits. For that reason, provision is made to synchronize the multivibrators with pulses of fixed repetition rate. Figure 26 shows that 2 mc clock pulses, amplified by the trigger tube (V3), are used for synchronization.

It is the function of the blocking oscillator to generate, in response to the control pulse, a clear pulse which returns all of the multivibrators to the normal condition. The choice of a blocking oscillator as a source for the clear pulse will be discussed later on. The purpose of the gate generator (V9 and V10) and the integrator (V11) is evident from the previous discussion.

The remaining parts of the block schematic of the conversion device are gate-and-delay units used here to form DE 1 and DE 2. As mentioned in an earlier part of this paper, a gate-and-delay unit is one

of the test-equipment panels designed and constructed by Project Whirlwind.[1] The unit provides an output pulse delayed in time up to several thousand microseconds with respect to the input pulse.

The physical form of the conversion device is shown in Figure 27, which is a photograph of the conversion device and the test equipment used in its operation. The two top panels make up the conversion device. The gate generator and integrator are constructed on the upper panel; the lower panel consists of delay elements 3 and 4 and the associated circuitry. The construction of the conversion devices follows the principles used throughout the Whirlwind computer: vacuum tubes, power connectors, and jacks for interconnections between units are mounted on one side of the aluminum panel, and circuit components are mounted on the other side with the aid of phenolic terminal boards. The photograph shows the component side of the conversion device. The test equipment used will be identified in Section 3.323, where a method of adjusting the multivibrators is described.

This section has been intended as a functional description of the conversion device. In the following sections, a more detailed description will be given and the design features will be discussed.

3.322 Circuit Designs

3.3221 The Multivibrators

In the design of the multivibrators, great care must be taken to achieve the most stable and jitter-free operation possible, for the success of this method of decoding depends more on the accuracy with which DE 3 and DE 4 can be made equal and constant than on any other single design factor.

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1. Ref. 12

Monostable multivibrators are well known.[1] For that reason, their basic principle of operation will not be described here. Instead, discussion will be limited to those considerations which led to the particular multivibrator circuits shown in Figure 28. Since all multivibrators are nearly alike, only one of them, multivibrator 1, will be described in detail. The points in which the multivibrators differ will also be discussed.

Recent literature[1] describes some of the practical considerations which lead to well-designed multivibrators. As in most trigger circuits, the choice of a tube to be used is guided by the realization that, in order to achieve rapid rise times, loading capacitances must be kept to a minimum and should be charged or discharged in the least possible time. This consideration requires the use of tubes with sharp cut-off characteristics, high current-carrying capacity, large transconductance, and low input and output capacitances. For these reasons, type 5687 tubes were here used. These are dual triodes of miniature construction. Pentodes are actually better suited for the generation of fast waveforms because of smaller input capacitances. However, pentodes require screen-voltage supplies and were not used here to eliminate the need for an additional voltage source.

The basic form of monostable multivibrator chosen is the most common one known. V1B is the normally-on tube and V1A the normally-off tube. The timing resistor (made up of the series arrangement of two 1 megohm resistors and a 25,000 ohm potentiometer) is returned to plate-supply

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1. Ref. 5., pp. 159-195

potential in order to have the greatest possible slope of the timing exponential at the instant when V1B conducts again. The larger the slope of the timing exponential when V1B is about to resume conduction, the more nearly fixed will be the instant of switchover in conduction from V1A to V1B, and the greater will be the stability of the delay interval.

The R-C timing network is made up of a relatively low capacitance and a high resistance. These parameters were chosen to achieve good recovery time. After the delay period is over, the timing capacitor recharges through the load resistance in the plate circuit of V1A and the clamping diode. Thus, to shorten the recovery time, the size of the timing capacitor and the plate-load resistor of V1A should be minimized. The time constant of the timing network is fixed by the amount of required delay (in this case, approximately 70 microseconds for each multivibrator, so that T_1 is 140 microseconds). With the small timing capacitor here used, a large timing resistor must therefore be used (over 2 megohms).

Considerations of recovery time have already shown that the plate-load resistor of V1A should be small. But in order to have the maximum possible slope of the timing exponential when the change of state from V1A conducting to V1B conducting occurs, it would be desirable to have a large drop in the plate-load resistor of V1A. This would call for a large plate-load resistor, thus contradicting previous considerations based on good recovery time. A compromise therefore has to be made, and 6,300 ohms was chosen as the value of the plate-load resistor for tube V1A.

The plate-load resistor of V1B, however, is not limited by the requirement for a large voltage swing at the plate of V1B. The voltage

swing at that point must merely trigger multivibrator 2, and the plate-load resistor may therefore be small, thus resulting in a steep waveform at the plate of V1B. This is highly desirable for triggering multivibrator 2. The lower limit of the value of the plate-load resistor of V1B is thus only limited by the maximum allowable plate dissipation of the tube. A 3,100 ohm resistor was therefore used.

Self-bias, provided by the cathode resistor, was chosen here in preference to a fixed bias in order to decrease the sensitivity of the circuit to changes in operating conditions. The cathode bias will counteract small changes in supply voltages and small variations in tube characteristics. For example, if the emission of the tube should drop slightly, the cathode bias will tend to decrease slightly and thereby compensate for the loss in tube emission.

In addition to stabilizing the operation of the tubes, the cathode resistor also assists in the switchover action. This multivibrator is therefore both plate-to-grid- and cathode-coupled. The values for the components in the plate-to-grid-coupling network and the proper value for the cathode resistor can be found readily from the plate characteristics of the tube by considering that when V1B is conducting, V1A shall be cut off and when V1A is conducting, its grid bias shall be slightly negative.

The purpose of the clamping diode (V7) is to set the grid potential of V1B, the normally-on tube, at a definite fixed potential, slightly negative with respect to the cathode. If clamping action were not employed, there would be grid-to-cathode current in V1B during the normal state because the timing resistor is returned to plate-supply potential. The result

of the grid current would be that the potential of the right-hand terminal of the timing capacitor would vary with the grid-to-cathode resistance of V1B and the cathode current of that tube. The left-hand terminal of the timing condenser is connected to plate-supply potential. Thus the voltage across the timing capacitor and hence the initial charge on it at the beginning of the delay period would vary with fluctuations in tube characteristics. The result of this would be undesirable variations in the delay period provided by the multivibrator. By clamping the grid of V1B to a fixed potential and not allowing the flow of grid current, the initial charge on the timing condenser is fixed and more stable operation results. Because of their low plate-to-cathode capacitance and low forward resistance, type 6AL5 diodes are used.

Brief mention should also be made of the purpose of the remaining components in the multivibrator circuit. Small resistors, arbitrarily chosen as 47 ohms, are inserted in series with the control grids to eliminate parasitic oscillations. Because type 5687 tubes have a very high transconductance, the presence of grid-to-plate capacitance often leads to high-frequency oscillations in the tube. These oscillations can be prevented by decreasing the Q of the grid circuit through the use of a small resistor.

The plate-supply potential is not applied directly to the plate-load resistors, but through a R-C filter network in order to decouple the multivibrators from each other. The filter is made up of the 22 ohm resistor and the parallel combination of a 0.1 and a 0.01 microfarad condenser. The 0.1 microfarad condenser, being of tubular construction, has considerable

inductance at high frequencies and would not give proper decoupling action for a steep waveform on the common plate-supply line. For that reason, a 0.01 microfarad mica condenser, having better high-frequency characteristics, is added.

Wire-wound resistors are used in several places because their stability is greater than that of composition-type resistors. The timing resistors need not be precision resistors of the type used here, but may have greater tolerance, providing they are sufficiently stable. The mica timing capacitors here used are JAN characteristic E. Here again the choice of components is based on maximum possible stability.

Attention will now be turned to the manner in which the multivibrators are triggered and interconnected. Trigger pulses of negative polarity arrive from DE 1 and DE 2 at J1 and J2, respectively. The trigger pulses are applied at the plates of the normally-off tubes, reaching the grids of the normally-on tubes through the timing capacitors. In order to remove the triggering sources from the multivibrators at all times except when the negative-going portion of the trigger pulse arrives, diodes are inserted in the triggering path. Because of their low inter-electrode capacitance and long life, germanium-crystal rectifiers are well suited for applications requiring fast waveforms and are used here. Since the rated back voltage of type D358 crystal rectifiers is 75 volts and in this circuit the voltage swing at the plates of the normally-off tubes is approximately 150 volts, two crystal rectifiers are used in series for each trigger path. In order to distribute the total back voltage of 150 volts equally across the two crystal rectifiers, the 220,000 ohm resistors in parallel with the crystal rectifiers are used.

The multivibrators trigger each other through the 12 micro-micro-farad coupling condensers. The value of the coupling condensers is quite critical, as the following discussion will show. Consider multivibrator 1. At the plate of the normally-on tube, there is a rectangular waveform, the positive-going edge occurring at the start of the delay period and the negative-going edge occurring at the end of the delay period. Multivibrator 2 should, of course, be triggered at the end of the delay period, and the coupling condenser must therefore be large enough so that the negative-going edge will trigger multivibrator 2. But if the coupling condenser is too large, the timing condenser of multivibrator 2 will charge through the clamping diode during the positive-going part of the waveform at the plate of V1B. When the plate waveform then reaches a steady value, the timing condenser discharges. Its discharge path consists of the 6,300 ohm resistor and the timing resistor. Since the upper end of the timing resistor is at a fixed potential, the lower end and hence the potential at the grid of V2B then drop in potential. Triggering of multivibrator 2 at an undesired moment can then occur. The upper limit for the value of the coupling condenser is thus fixed by the need to prevent unwanted triggering of multivibrator 2 from occurring, and the lower limit is set by the requirement that the negative-going edge of the waveform at the plate of V1B trigger multivibrator 2. The value of 12 micro-microfarads for the coupling condenser was determined experimentally.

The required trigger pulse for the gate generator at the end of the delay period of multivibrator 2 is formed by the ringing circuit in the plate circuit of V2B. The ringing circuit, an underdamped R-L-C

combination, is formed by the 100 microhenry choke and the existing stray capacitance. The D357 crystal rectifier removes the positive half of the ringing signal after the initial negative half-sinusoid and dissipates all energy, thus preventing further oscillations. A single negative-going pulse is thereby generated at the end of the delay period of multivibrator 2. A photographic picture of this output pulse is shown in Figure 31(a). The pulse is seen to have a duration of approximately 0.3 microsecond and an amplitude of approximately 25 volts.

3.3222 Clearing of the Multivibrators

Since new information may be furnished by the computer to the decoder at any time, provision must be made to clear the multivibrators, i.e., return them to the normal state, regardless of the instantaneous condition of the R-C timing network. Therefore, before a new control pulse arrives at J1, a pulse must be available which causes the right-hand tubes of all the multivibrators (V1B, V2B, V5B, and V6B) to conduct. This clear pulse is provided by the blocking oscillator (V4). We recall from the block schematic, Figure 26, that the input to the blocking oscillator is the actual control pulse from the computer; the input to J1 is that same pulse, but delayed in DE 1.

The blocking oscillator uses a type 2C51 double triode, the first section serving as a trigger tube and the second one as the actual blocking oscillator. The circuit arrangement follows a common form.[1] At the present state of the art, there is no analytical approach to the design of blocking

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1. Ref. 5., pp. 205-238

oscillators because of non-linearities in the tube and the pulse transformer. Parameters used in this blocking oscillator were therefore derived by a process of trial and error.

The output pulse from the blocking oscillator reaches the normally-off tubes of all the multivibrators (V1A, V2A, V5A, and V6A). The pulse is of negative polarity and by cutting off all the normally-off tubes, it assures that the normally-on tubes are made to conduct and hence brings about the clearing action. Because clearing at the desired instant must occur regardless of the instantaneous condition of the timing condensers, a relatively long clear pulse of large amplitude is required. A photographic picture of the clear pulse is shown in Figure 29(a). The pulse is seen to be approximately 1.2 microseconds long, with a maximum amplitude of 53 volts. The clear pulse is applied to the grids of the normally-off tubes through type D357 crystal-rectifier diodes. These isolate the four multivibrators from each other and also remove the loading effect of the blocking oscillator on the multivibrators.

The clearing action is shown in Figures 30(a) and (b). Before discussing these waveforms, it may be well to review the method in which the multivibrators operate.

Consider multivibrators 3 and 4, which make up DE 4. Assume that the multivibrators have been cleared, i.e., tubes V5B and V6B conduct. Upon arrival of the information pulse, V5A is made to conduct and V5B is turned off. After 70 microseconds, V5B resumes conducting and V5A is cut off. This is the first part of the delay which makes up the total delay in DE 4. When V5B resumes conducting, multivibrator 4 is triggered,

V6B is cut off, and V6A conducts. After another 70 microseconds,* V6B resumes conducting, and a trigger pulse, delayed 140 microseconds with respect to the information pulse, is sent to the gate generator. At the same time, multivibrator 4 triggers multivibrator 3, and the previous action is repeated, with the trigger from multivibrator 4 taking the place of the original information pulse.

Figure 30(a) illustrates this action. In that figure, a photographic picture of the waveform at the cathodes of V6A and V6B is shown. (The cathode waveforms of all multivibrators are the same in shape.) Because the tubes have unequal plate-load resistors, the cathodes are at the higher potential when V6B conducts and at the lower potential when V6A conducts. Thus the lower potential in the waveform of Figure 30(a), corresponding to V6A conducting, indicates the period during which multivibrator 4 contributes its delay to the total delay in DE 4; the higher potential in the waveform of Figure 30(a), corresponding to V6B conducting, indicates the period during which multivibrator 3 contributes its delay to the total delay in DE 4. At every positive-going edge in the waveform, the gate generator and multivibrator 3 are triggered; at every negative-going edge, multivibrator 4 is triggered.

Figure 30(b) shows the clearing action. A clear pulse is applied to the multivibrators approximately 10 microseconds after the start of the waveform. Comparison with Figure 30(a) shows that V6B is thereby

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* It is, of course, not necessary that the delays in multivibrators 3 and 4 be equal. The system only demands that the total delay in DE 3 be exactly equal to the total delay in DE 4. For a more complete discussion of this point, see Section 3.3233.

made to conduct at an earlier time, and multivibrator 4 is brought into its normal state. When the new information pulse arrives at J2, it triggers multivibrator 3, but leaves multivibrator 4 in the normal state. The occurrence of the new information pulse (here 40 microseconds after the clear pulse) can be seen by the small negative dip in the waveform of Figure 30(b). (The small dip is caused by the action previously described in the discussion of the determination of the proper value for the coupling condenser between the multivibrators.) Multivibrator 4 remains in the normal state until 70 microseconds after the arrival of the new information pulse. At that time, multivibrator 4 is triggered and V6A conducts. After another 70 microseconds, V6B again becomes conducting, multivibrator 3 and the gate generator are triggered, and operation identical with that previously described in connection with Figure 30(a) occurs.

3.3223 Synchronization of the Multivibrators

The need for maintaining accurate and identical delays in DE 3 and DE 4 has already been stressed. The multivibrators are made to meet that requirement by the use of 2 mc synchronising pulses.

Synchronizing a multivibrator consists of superimposing upon the timing exponential positive pulses which will increase the slope of the exponential at the occurrence of a synchronising pulse and thereby bring about the change of state at the instant of application of a particular synchronizing pulse. This action removes the small uncertainty as to the exact moment of change of state which would exist if no external synchronization were applied.

Synchronization is here brought about by injecting into the grids of the normally-off tubes negative pulses derived from the trigger tube, V3. (See Figure 28.) During the delay period of a multivibrator, the normally-off tube is conducting. The negative synchronizing pulses will therefore decrease the conduction of the normally-off tube and thus cause positive pulses to appear at the plate of the normally-off tube. These positive pulses are superimposed on the timing exponential and the desired synchronizing action is thus accomplished.

Figure 30(c) shows the synchronizing effect. The lower level of the waveform at the cathode of a multivibrator, which, as we have already seen, occurs during the delay period, shows small negative dips. These indicate that the conduction of the normally-off tube is decreased by the synchronizing pulses. Shortly after a particular synchronizing pulse the change of state occurs, which is here indicated by the rise in cathode potential. The change of state does not occur directly when the synchronizing pulse is applied because switchover does not occur instantaneously.

As a source of synchronizing pulses, a clock-pulse generator[1] of the type previously mentioned was used. The output of the clock-pulse generator is fed to J3 of Figure 28. V3 then supplies the amplified synchronizing pulses to all the multivibrators. The synchronizing pulses are connected to the grids of the normally-off tubes through 5 micro-microfarad condensers. These condensers are small enough to allow all

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1. Ref. 9

the multivibrators to be connected to the same point (the plate of V3) without interaction among multivibrators occurring. A very simple and economical synchronizing circuit thus results.

Figure 29(b) shows the input to the trigger tube, V3. The pulses at that point are nearly 0.1 microsecond long and have an amplitude of approximately 25 volts. The grid circuit of the tube clamps the top of the input waveform at zero potential by building up a negative bias on the 0.001 microfarad coupling condenser. The cut-off voltage of the type 5687 tube with the given plate-supply potential of 250 volts is -22 volts. Thus, because of the clamping action in the grid circuit, the base line of the input waveform is well below cut-off and small changes in the amplitude of the input pulses do not affect the output of V3. As long as the amplitude of the input pulses is greater than 22 volts, the plate waveform of V3 remains unaffected. This is a valuable feature in the operation of the multivibrators, since it means that the synchronizing action is not affected by small variations in the amplitude of the synchronizing input to J3.

The waveform at the plate of V3 is shown in Figure 29(c). The output of V3 does not follow the shape of the input waveform for the following reasons. At the occurrence of an input pulse to V3, the tube is made to conduct and the capacitance at the plate of V3 charges rapidly. The rapid linear fall in the plate waveform thus results. In the interval between synchronizing pulses, the capacitance discharges slowly through the 3,900 ohm plate-load resistor; the slow rise in the plate waveform thus results.

At this point, it may be well to re-examine the over-all operation of the multivibrators with the aim of further clarifying the timing relationships.

The previously established requirement that the decoder be accurate to 1 part in 256 means that, because each of the delay elements 3 and 4 provides delays somewhat greater than 128 microseconds, these delays must be accurate within 1/2 microsecond, or within the time interval between two successive synchronizing pulses.. We can now see how synchronization brings about operation which is accurate within that limit.

Consider the information pulse. As we have seen, it may arrive at any time. This means that at the end of the first delay in multivibrator 3, the change of state may coincide with one of two possible synchronizing pulses. The first delay may, therefore, differ from the design value by 1/2 microsecond in the worst possible case. Thus the very first delay takes up all the allowable tolerance, and no further deviations from the desired delays must occur. No additional errors are actually introduced as the information pulse "circulates" in DE 4, because after the very first delay in multivibrator 3, all triggering coincides with a synchronizing pulse. By the very nature of synchronization, a multivibrator will always change its state after a fixed number of pulses, providing it has been triggered in coincidence with a synchronizing pulse. In our example, the first output pulse from multivibrator 3 occurs simultaneously with one of two possible synchronizing pulses, but the trigger nevertheless is coincident with a synchronizing pulse. Therefore, the first output pulse from multivibrator 4 surely occurs after a fixed number of synchronizing

pulses. Similarly, because the output of multivibrator 4 is coincident with a synchronizing pulse, the second output pulse from multivibrator 3 occurs after a fixed number of synchronizing pulses. The same action continues as long as the information pulse "circulates" in DE 4. Thus we see that the only possible source of error occurs in the very first delay in multivibrator 3. Accuracy demands are therefore fulfilled.

3.3224 The Gate Generator

The remaining parts of the conversion device are the gate generator and the integrator. The circuit schematic of these components is shown in Figure 32. The gate generator consists of a flip-flop developed by Project Whirlwind. The design will therefore not be discussed here in detail and only the functional operation will be described.

The flip-flop is so arranged that the plate of a non-conducting tube is at nearly ground potential, while the plate of a conducting tube is at approximately -40 volts. The output terminal of the flip-flop (the point at which the control grid of the integrator tube is connected) can be at one of two possible potentials: nearly ground (when V10 is cut off) and approximately -17 volts (when V10 is conducting). A negative pulse from DE 3 will cut off V10, thereby generating the positive-going edge of the gate waveform. A negative pulse from DE 4 will cut off V9 and turn on V10, thereby generating the negative-going edge of the gate waveform. Reference to Figure 25 shows that this is the desired operation.

Figures 31(b) and (c) are photographic pictures of the waveforms at the output of the gate generator. Figure 31(b) is the waveform resulting when the number 0 is decoded. Previous discussion might have led one to

expect that the gate length corresponding to the number 0 would be 1/2 microsecond. (We recall that to obtain the information pulse from the binary counter, it takes one more pulse input to the counter than the number to be decoded. We have here assumed that the repetition rate of the counter input is 2 million per second. Hence, when the number 0 is decoded, it will take 1/2 microsecond to obtain the information pulse.) Figure 31(b) shows that the gate length is 1 1/2 microseconds. This was brought about here deliberately by making the delay in DE 2 longer than the delay in DE 1 in order to avoid possible errors in the operation of the gate generator. If the pulses from DE 3 are nearly coincident in time, the flip-flop may not trigger as desired and erroneous gate lengths may result. By making the delay in DE 2 longer than that in DE 1, it is certain that simultaneous or nearly simultaneous triggering at both inputs to the flip-flop cannot occur. Faulty operation will then never result.

It might now be thought that the "misadjustment" of DE 2 will cause inaccurate operation, since the number 0 will no longer result in zero output from the decoder, and all other numbers will produce proportionately larger outputs. Strictly speaking, this is true. But the shift in output level brought about by making DE 2 longer than DE 1 is only a matter of calibration. The number 0 will still result in a unique output level, although that level is no longer 0. Similarly, all other numbers will still have corresponding output levels, and it only remains to make allowance for the small shift in all the levels.

This may appear a bothersome problem. But actually it is not of any practical significance, since some provision must always be made

to add to the output of the decoder some kind of a zero adjustment. Up to now, we have spoken of decoding numbers ranging from 0 to 255. In practical applications, it will be necessary to decode negative as well as positive numbers. But the decoder has no provisions for differentiating between negative and positive numbers. In order to overcome this difficulty, the computer will add to all the numbers to be decoded a positive constant equal to the magnitude of the largest possible negative number, thereby allowing the decoder to operate with positive numbers only. However, the voltage-amplitude input to the controlled channel must be positive as well as negative, depending on the sign of the original number to be decoded. For that reason, a voltage amplitude corresponding to the positive constant added by the computer must be subtracted from the output of the decoder.* We can now see that the shift in calibration brought about by "misadjusting" DE 2 is of no practical significance; it is taken care of by proper adjustment of the constant voltage subtracted from the output of the decoder.

Figure 31(c) shows the output of the decoder corresponding to the maximum number (255) being decoded. The delays in DE 3 and DE 4 are made 12 microseconds longer than the maximum time interval between the control and information pulses. For that reason, even when the maximum number is being decoded, the output pulses from DE 3 and DE 4 can never coincide and simultaneous triggering of both inputs to the gate generator is thus avoided. The short gaps in the waveform of Figure 31(c) illustrate this point.

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* This point will be discussed again in Section 3.52.

3.3225 The Integrator

The purpose of the integrator is to provide an output voltage which is proportional to the average level of the series of gates applied to the input of the integrator. Integration is here accomplished by feeding a R-C network from a constant-current source.

A type 6AU6 pentode serves as the constant-current source. The plate characteristics of that tube are very flat above the knee, and operation above this point thus assures that the tube operates as a nearly-ideal constant-current source. The tube has a very sharp cut-off characteristic and, with the supply voltages here used, cut-off occurs with a control-grid potential of somewhat less than -3 volts. Since the lower level of the output of the gate generator (-17 volts) drives the tube well below cut-off, it conducts only during the positive part of the input waveform. A series of current gates is thus fed to the R-C plate load where the integration occurs.

The parameters for the R-C network are determined by the following considerations. In order to have a large output voltage across the R-C network, the value of resistance used shall be as large as possible. The maximum value of resistance is fixed by the requirement that the tube operate above the knee of the plate characteristics. A value of 18,000 ohms for the resistor was thus arrived at. This gives a maximum output voltage of 53 volts. The time constant of the R-C network must be much larger than the time between successive gates at the input to the integrator (140 microseconds) and much smaller than the minimum time between successive pieces of information furnished to the decoder by the computer. Of course,

the time between successive read-out operations by the computer is determined by the particular application considered and cannot be fixed uniquely. As a typical figure, it was assumed that the computer supplies new information every 20 milliseconds. The time constant of the R-C network was therefore made 1.8 milliseconds, which is nearly 13 times the interval between successive gate inputs to the integrator and about 1/11 of the time between successive readings to the decoder. In Section 4, more will be said about the network in the integrator.

3.323 Alignment Procedure

Once again, it is recalled that the success of the method of decoding described here depends on the degree with which DE 3 and DE 4 can be made to be equal. One cannot expect the four monostable multivibrators which make up DE 3 and DE 4 to perform identically, unless adjustments are provided to make compensations for variations of the tubes and other components from the nominal ratings. In the circuit of the multivibrators (see Figure 28), variable condensers (the Erie ER300 trimmers) and the 25,000 ohm potentiometers are provided for the purpose of adjusting DE 3 and DE 4 for exactly equal delays. The adjustments of these components are highly critical and may, at first, seem intricate. An orderly procedure for adjusting the multivibrators is therefore necessary. The procedure to be described in Section 3.3233 has been found simple and efficient. It can be carried out in a matter of minutes. Before giving the details of the procedure used, a general description of the test setup required is in order.

3.3231 Test Equipment

Because most of the test equipment shown in Figure 33 is unusual and was specially designed by Project Whirlwind, a brief description of all non-commercial units is given.

(1) Pulse Standardizer.[1] The purpose of this unit is to provide at the output a standard pulse for each positive input pulse. The amplitude and shape of the output pulse is entirely independent of the input pulse. A standard pulse has a duration of 0.1 microsecond and its shape approximates that of a half-sinusoid.

(2) Gate-and-Delay Unit.[2] This unit provides a standard-pulse output delayed with respect to the positive input pulse by a time interval which is continuously variable from 0.5 to 2500 microseconds.

(3) Multivibrator Frequency Divider.[3] As used in this application, the multivibrator frequency divider steps down the repetition rate of the input pulses to a repetition rate which can be varied from 60 cycles to 200 kc. Division is accomplished in two cascaded stages. The output of the first divider stage is available in the form of standard pulses at the terminal marked "standard pulse output". The output of the second divider stage (marked "output") is a large, negative, non-standard pulse designed primarily to trigger the sweep of a type P5 synchroscope. The output pulse from the second divider stage can be delayed by a variable amount. In this setup, the output pulses will be in synchronism with the source connected to the terminal marked "input to lock-in delay".

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1. Ref. 11
2. Ref. 12
3. Ref. 33

3.3232 Interconnections of the Test Equipment

The interconnections of the test equipment will now be discussed. The 2 mc clock, described in Section 3.3223, is the primary source of pulses. Its output reaches J3 of Figure 28 through the upper pulse standardizer of Figure 33, thus synchronizing the multivibrators. The output of the clock is also supplied to the multivibrator frequency divider, which triggers the sweeps of both the type P5 synchroscope and the Tektronix oscilloscope. The trigger output of the P5 synchroscope, after shaping in the lower pulse standardizer of Figure 33, is fed into both gate-and-delay units. The two gate-and-delay units then provide two pulses which serve to simulate the control pulse and the information pulse. The output of the right-hand gate-and-delay unit triggers multivibrator 1 (J1 of Figure 28) and that of the left-hand gate-and-delay unit triggers multivibrator 3 (J2 of Figure 28).

To summarize the operation of the test setup shown in Figure 33, we see that the sweeps of both the P5 synchroscope and the Tektronix Oscilloscope, as well as the timing of the multivibrators in the conversion device, are synchronized with 2 mc pulses. For every sweep of the P5 synchroscope, and in synchronism with that sweep, all multivibrators are cleared and furnished simulated control and information pulses. The time interval between the control pulse and the information pulse is varied by manually adjusting the gate-and-delay units. Note that with this setup the gate-and-delay units also serve as DE 1 and DE 2 of Figures 24 and 26. This is accomplished by making the delay in the right-hand gate-and-delay unit equal to the required value for DE 1; the delay in the left-hand gate-and-delay unit is adjusted to be the sum of the delay in DE 2 and the time interval between the control pulse and the information pulse.

With this setup, the deflection plates of the P5 synchroscope may be connected to any point in the conversion device and any desired measurements may be taken.

3.3233 The Adjustments of the Multivibrators

Let us now return to the procedure for adjusting the multivibrators of the conversion device. The aim in adjusting the multivibrators is to make DE 3 and DE 4 equal. At first, it may seem that it does not matter at all how the total delays in DE 3 and DE 4 are apportioned among their respective multivibrators. While this is true to some extent, it is harmful to make the delay provided by any one multivibrator very much different from that provided by its mate. In view of the previously established specifications (see Section 3.321), a good value for the total delay in DE 3 and DE 4 is 140 microseconds. One could arbitrarily set the delay in multivibrator 1 for 40 microseconds and that in multivibrator 2 for 100 microseconds. This would be a poor procedure, for the timing exponential of one multivibrator would be much longer than that in the other. For a given synchronizing frequency, the longer the timing exponential, the poorer the synchronization achieved. We can now see that by making the multivibrators very much different, unbalance has been created and the chances for faulty operation have been increased. For that reason, it is best to make the delays in all the multivibrators equal. Of course, no special effort need to be made in order to achieve exact similarity in all multivibrators. It is perfectly safe to make the delay in one multivibrator 68 microseconds and that in its mate 72 microseconds. For the sake of simplicity, we will speak of making all individual delays 70 microseconds;

it is understood that small deviations are permissible, providing the total delay in DE 3 equals that in DE 4.

The adjustments of the multivibrators are carried out in two steps: the "rough" adjustment and the "fine" adjustment. In the rough adjustment, only the trimmer condensers (5-20 MMFD, Erie MR300) of Figure 28 are used. The 25,000 ohm potentiometers in the timing circuit are set to their center position from which they are not moved until the fine adjustment is to be made.

The rough adjustment consists of observing the multivibrator waveshapes and setting the trimmer condensers so that the delay in each multivibrator will be 70 microseconds. A convenient point for observing the waveform is the cathode of the multivibrator tubes. The waveform at the cathodes will be as shown in Figure 30(c). A count of the number of small negative dips caused by the synchronizing pulses will indicate accurately the length of the delays provided by the multivibrators. Since the desired delays are 70 microseconds and the synchronizing pulses occur every 0.5 microsecond, the proper count of small dips is 140. Counting so large a number of pulses is a tedious task. For that reason, marker pulses obtained from the multivibrator frequency divider (terminal marked "standard pulse output") are connected to the lower deflection plate of the Tektronix oscilloscope. By proper adjustment of the multivibrator frequency divider, one marker can be made to appear for every 8 or 10 synchronizing pulses. Thus the counting procedure is greatly simplified and it can be carried out quickly and easily. (The Tektronix oscilloscope is used here because it has a sweep magnifier, i.e., portions of the cathode

waveform can be selected at will for observation. The counting procedure is thereby simplified, since the entire cathode waveform can be made to "move" along the face of the cathode-ray tube by manual control. As the display "moves" along, the markers and the synchronizing pulses are counted.)

Although the above adjustment provides an exact measure of the delay, it is made under the condition where the oscilloscope loads down the multivibrator circuits. When the oscilloscope leads are removed, the delays will be slightly different. It is the purpose of the fine adjustment to compensate for the loading effect of the oscilloscope.

With the type P5 synchroscope connected to the output of the gate generator and no test equipment connected to the multivibrators, one should observe a series of equal gates for each pair of pulses supplied to the conversion device. With only the rough adjustment made, the length of the gates will vary with time, and hence a blurred picture will result. The 25,000 ohm potentiometers are now adjusted until a series of equal gates is shown on the face of the oscilloscope. There is no simple sequence for carrying out the fine adjustment and one simply has to turn the potentiometers until the desired result is obtained. This may at first seem a tedious process, but the loading effect of the oscilloscope during the rough adjustment is very small. Before the fine adjustment is made, the settings of the multivibrators are nearly alike and do not require much change. For that reason, the potentiometers are made sufficiently small so that they can change the delays by only 1 microsecond. The fine adjustment does not require more than a few minutes.

3.4 RESULTS OBTAINED

3.41 Delay Elements 1 and 2

Experimental results show that DE 1 must provide a minimum delay of 3.2 microseconds. This is a very reasonable value, since the time constant of the recharging path of the timing condenser is approximately 0.9 microsecond. (See Section 3.3221.) For the reasons discussed in Section 3.3224, it is desirable to make the delay in DE 2 somewhat greater; a minimum value of 4.2 microseconds is useful. With these adjustments, the time interval between the clear pulse and the new trigger pulses applied to the multivibrators (Figure 28) is sufficiently long to result in satisfactory operation. Clearing may then occur at any time and the time relationship between the control and information pulses is not distorted as these pulses are "circulated" in DE 3 and DE 4.

Because DE 1 and DE 2 must furnish delays of only 3.2 and 4.2 microseconds, respectively, passive electrical delay lines may be used in their design. The stability and reliability of electrical delay lines is excellent and no trouble should be encountered in their application.

We recall that test equipment constructed by Project Whirlwind was used in this investigation for DE 1 and DE 2. When special units incorporating commercially available delay lines are built for DE 1 and DE 2, the output pulses from these units, which trigger multivibrators 1 and 3, should be made somewhat wider than 0.1 microsecond. It was observed that when 0.1 microsecond pulses are used to trigger the multivibrators, a minimum pulse amplitude of 27 volts is required. The required pulse amplitude can be reduced by increasing the width of the trigger pulses,

since thereby no reduction in total pulse energy occurs. A good value for the width of the output pulses from DE 1 and DE 2 is approximately 0.5 microsecond.

We can now see why good recovery time of the multivibrators was considered important in Section 3.3221. By making the time constant of the recharging network of the timing condenser small, the required delays in DE 1 and DE 2 are sufficiently short to allow the use of electrical delay lines, which are the simplest and most reliable devices of their class.

3.42 Accuracy

Measurements of the accuracy of the decoder were made in two ways: (1) by "circulating" in DE 3 and DE 4 a pair of pulses of known time relationship and measuring the time relationship maintained by the pulses during the course of the "circulating" action, and (2) measuring the output of the conversion device corresponding to a known input.

The results of the first test are presented in Table 3.1. The time interval between the input to DE 1 and the input to DE 2 is shown in one column; in the other, the corresponding time interval held by the multivibrators is given. We note that the time interval in the second column is either 1 or 1.5 microseconds longer than that in the first column. We can account for 1 microsecond of that difference by the fact that DE 2 was intentionally set for a delay which was 1 microsecond longer than that in DE 1. Thus, for coincident inputs to DE 1 and DE 2, the time interval held by the conversion device was 1 microsecond. The additional 0.5 microsecond by which the two columns of Table 3.1 differ at some points

TIME INTERVAL BETWEEN INPUT TO DE 1 AND INPUT TO DE 2, microseconds	TIME INTERVAL HELD BY CONVERSION DEVICE, microseconds	TIME INTERVAL BETWEEN INPUT TO DE 1 AND INPUT TO DE 2, microseconds	TIME INTERVAL HELD BY CONVERSION DEVICE, microseconds
0	1	65	66
2.5	4	67.5	68.5
5	6	70	71
7.5	8.5	72.5	74
10	11	75	76
12.5	14	77.5	79
15	16.5	80	81.5
17.5	18.5	82.5	83.5
20	21	85	86
22.5	23.5	87.5	88.5
25	26	90	91
27.5	28.5	92.5	94
30	31	95	96.5
32.5	33.5	97.5	98.5
35	36	100	101
37.5	38.5	102.5	103.5
40	41	105	106.5
42.5	43.5	107.5	109
45	46	110	111
47.5	48.5	112.5	114
50	51	115	116
52.5	53.5	117.5	118.5
55	56	120	121.5
57.5	58.5	122.5	123.5
60	61	125	126
62.5	63.5	127.5	128.5

TABLE 3.1

is attributable to the synchronizing action previously described in Section 3.3223. We have seen there that, because of the synchronizing action, the time relationship between the control pulse and the information pulse can be distorted by 0.5 microsecond, but not by more. Table 3.1 gives experimental verification and proves that the "circulating" action does not introduce an error which is larger than 1 part in 256. Table 3.1 also shows that the error of 0.5 microsecond occurs at random points. Again, this is to be expected, since new control and information pulses were supplied to the conversion device at random moments.

The over-all accuracy of the conversion device was determined by supplying to the input pairs of pulses, the time interval between which was accurately known, and recording the corresponding output voltage of the integrator. Once again results were very good. A plot of the input-output characteristic would be a nearly-straight line and would not show the errors clearly. For that reason, only the error versus time interval between control and information pulses was plotted. Figure 34 shows the plot. We see that only three readings fall outside the $\pm$ 0.4 percent error lines. These errors are probably due to experimental techniques (e.g., inaccuracy in reading the voltmeter at the output of the conversion device) and can be disregarded. The over-all accuracy run was repeated twice, and again a few readings (2 in one case and 3 in the other) fell outside the $\pm$ 0.4 percent error lines. These errors were never greater than $\pm$ 0.6 percent and were never read at the same points. One is therefore justified in concluding that the conversion device has an accuracy of $\pm$ 0.4 percent, corresponding to $\pm$ 1 part in 250.

The tests described above were made under static conditions. A pair of pulses was supplied to the input of the conversion device and the corresponding output voltage was measured. Next, the time interval between the input pulses was manually varied and again the corresponding output was recorded. Section 4 will describe some dynamic tests.

3.43 Stability

It was observed that when a single pair of pulses was supplied to the input of the conversion device, the pair of pulses could be kept "circulating" in DE 3 and DE 4 for periods up to 5 hours. With the unit properly adjusted, it was always possible to maintain a pair of pulses for more than 5 minutes. In actual operation with the computer, the conversion device will never be required to hold information for so long a period and we can therefore conclude that the stability of the conversion device is better than required.

Some indication of the stability can be gained from Figures 31(b) and (c) which are photographs of the output waveform of the gate generator, made with an exposure time of approximately 4 seconds. Note that no jitter whatsoever is shown, even in Figure 31(b) which was taken with a synchroscope sweep-speed of 0.85 microsecond per inch. It was observed that the multivibrators have less than 0.02 microsecond jitter when no synchronizing pulses are applied. With synchronizing pulses applied, no jitter whatsoever could be observed with the P5 synchroscope.

3.44 Reliability

A complete determination of the reliability characteristics of the conversion device would require several weeks and was therefore not

made in this investigation. However, the operation of the unit was observed over several long periods of time. It was found that the conversion device requires small adjustments (carried out by changing the settings of the 25,000 ohm potentiometers of Figure 28) after 5 to 8 hours of operation. Only once could the unit be operated for 17 hours without the need of making any adjustments.

The reliability is therefore not fully satisfactory. In practical applications of the decoder, it should not be necessary to adjust the unit more than once daily. However, it is believed that the design developed here is capable of more reliable operation. In Section 3.61, methods will be suggested which are expected to result in greater reliability and the realization of the ultimate design goal, which is reliable operation over a 24 hour period.

3.45 The Critical Parameters

In circuits where only on-off types of signals are used, small variations of circuit parameters are not harmful. This is the great advantage of on-off operation. In on-off operation, the exact amplitude of a pulse or its precise timing do not matter. As long as the pulses are such that their presence or absence can be detected, operation will be fully satisfactory. However, in circuits such as the conversion device described here, the exact nature of the signal is important. Small changes in circuit parameters can then introduce errors. In our case, information is held in the form of a time interval between two pulses. If that interval is varied somewhat during the holding process, erroneous outputs result. Thus the conversion device does not have the relatively wide margin of

operation inherent in on-off operation. This is to be expected, since the purpose of the decoder is the conversion of binary numbers (essentially on-off signals) to voltage amplitudes (analog quantities the exact magnitude of which carries the information). Up to the integrator, the conversion device holds information in the form of a time interval. Time has been chosen here as the domain in which to hold information, because electronic circuits are better suited for operation in the time domain than in the voltage- or current-amplitude domain. But still, the decoder is, by necessity, an analog device and must therefore suffer from the inherent disadvantage of analog devices, i.e., sensitivity to variations in circuit parameters.

Three of the supply voltages used in the design of the conversion device are critical: the plate-supply voltage of the multivibrators, the screen-grid voltage of the integrator tube , and the filament voltages. It was found that the plate-supply voltage of the multivibrators must not vary by more than $\pm$ 1 volt. The variations in screen-grid potential of the integrator tube should be kept to a minimum, since the plate current of a pentode is determined by the screen-grid voltage and not by the plate-supply voltage in operation above the knee of the plate characteristics. The filament voltages of all tubes should be well regulated. Plate current is still affected by filament voltage even when operation is space-charge limited due to the dependence of electron velocities on filament voltages.

The multivibrators of Figure 28 are sensitive to variations in the amplitude of the synchronizing signal applied to the grids of the normally-off tubes. This effect has been minimized here by the clamping

action in the grid circuit of the trigger tube (V3 of Figure 28). The manner in which the clamping action is accomplished has been discussed in Section 3.3223. Measurements show that the amplitude of the synchronizing signal input to the conversion device may vary by 3 volts without failure in operation occurring. This is believed to be a sufficiently wide margin.

3.5 EVALUATION OF THE DECODER

3.51 Accuracy

The accuracy which was achieved with this design will probably be satisfactory in many applications. There may be cases where higher accuracies are desired, and the question arises if the accuracy of the decoder investigated here can be improved.

The error introduced by the multivibrators of the conversion device can be expressed as

$$E = \frac{1}{f_c \times T}$$

where f_c = synchronizing frequency

T = maximum time interval between control pulse and information pulse.

The parameters used in this investigation are f_c = 2 mc, T = 128 microseconds. Thus, for our case

$$E = \frac{1}{2 \times 10^6 \times 128 \times 10^{-6}} = \frac{1}{256} = 0.391\%.$$

There are two possible ways of reducing the error caused by the multivibrators: increasing T and increasing f_c. Since T is the time interval

between the first pulse admitted to the counter and the appearance of the counter end-carry pulse in the case of the maximum number to be decoded, increasing T means that the binary counter will be connected to each output channel for a longer period of time. A reduction in the number of channels which share a given counter will thus result. We have previously seen that with the parameters used here, the binary counter may be shared by 150 channels. In practical applications, so large a number of channels may not be necessary. It therefore appears that it is feasible to increase T. As T is increased, T_1 (Figure 25) must also be increased. But there is a limit to the amount of delay which the multivibrators can furnish accurately, since the slope of the timing exponential decreases as the delay period increases. In this application, each multivibrator provides a delay of 70 microseconds, which is approximately 1/3 of the time constant of the timing exponential. Operation was thus restricted to the region where the timing exponential is quite steep. If it is desired to increase T, care must be taken not to operate the multivibrators in the region where the slope of the timing exponential is small. In order to operate each multivibrator in the desired region and still increase T (and hence T_1), it may become necessary to add a third multivibrator in both DE 3 and DE 4. In that case, each multivibrator would supply only 1/3 of the total delay required.

The other method by which E, the error introduced by the multivibrators, can be decreased consists of increasing the synchronizing frequency. Here the possibilities are quite limited. The greater the number of synchronizing pulses superimposed on a given timing exponential, the

greater the uncertainty in the exact moment at which the change of state of the multivibrator occurs. Also, the various stray capacitances in the circuit and tube limitations make operation at higher synchronizing frequencies difficult. It was found that the multivibrators could not be synchronized with 4 mc pulses; the use of 3 mc pulses seemed possible, but it was not proven conclusively that fully satisfactory operation can then be obtained.

We conclude that the accuracy of the decoder can probably be increased somewhat. Just where the limit lies depends on the number of multivibrators used and, of course, the accuracy of the integrator stage.

3.52 The Output Stage

It is noted that in the operation of this decoder, pulses and gates of fixed amplitude are used up to the very last stage. Operation is thus confined to the time domain as much as possible. The output stage, the integrator, is a very simple circuit, consisting of a constant-current source and an integrating network or low-pass filter. With the parameters used here, the output signal corresponding to the maximum number has an amplitude of 53 volts. Thus in many applications no further amplification will be necessary and the chances for the introduction of additional inaccuracies are reduced. Of course, it may be necessary to use a filter in the output of the decoder which is better than the simple R-C network used here. The filter network used in an actual application will be determined by the over-all characteristics of the controlled system.

In Section 3.3224 we have seen that at the output of the decoder provision must be made for subtracting a fixed voltage corresponding to

the intentional "misadjustment" of DE 2 and the positive constant added by the computer to all numbers before they are decoded. No additional inaccuracies are expected from this step, since a voltage can be accurately set to 1 part in 1,000.[1]

3.53 Simplicity of Design

Simplicity of design is always desirable, not only from the point of view of economy, but also on the basis of the realization that the potential reliability of an electronic device is intimately related to the number of components used, particularly vacuum tubes.

Reference to Figures 28 and 32 shows that, in addition to clamping diodes, 14 vacuum tubes in 9 envelopes are used. To obtain a complete count of vacuum tubes required for this decoder, we must add to these figures the number of tubes used in DE 1, DE 2, and the binary counter. If electrical delay lines are used for DE 1 and DE 2, no more than 2 tubes (pulse amplifiers) should be required for each of these units. The binary counter must have 8 stages. Allowing 4 tubes for each stage, a total number of 32 tubes is required for the counter. If the counter is shared by a sufficiently large number of stages, the number of counter tubes per output channel is less than 1. We will assume that the counter adds one more tube to each decoder. The total number of tubes required by each decoder is therefore 19. This is a low number, considering the accuracy which the decoder achieves. By way of comparison, one might mention that a binary-weighted decoder of comparable performance would employ at least 32 tubes plus an output amplifier.

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1. Ref. 35., pp. 548-555

3.6 SUGGESTIONS FOR FUTURE WORK

3.61 Redesign of Delay Elements 3 and 4

Attention has already been called to the fact that the reliability of the conversion device is not sufficient. Efforts must therefore be made to achieve better reliability.

With the particular physical layout used in this investigation (see Figure 27), it was found that the multivibrators have a tendency to interact through electrostatic coupling. It is therefore recommended that in a future construction the multivibrators in DE 3 be shielded from those in DE 4. An improvement in reliability can be expected from a shielded construction.

This investigation has also revealed that type 5687 tubes are not fully reliable. At one time intermittent operation resulted from a 5687 tube which had unstable characteristics. While this particular tube was acceptable on the basis of rigorous static tests to which all tubes used by Project Whirlwind are subjected, in this application the variations in tube characteristics caused intermittent operation. As we have already seen, margins of operation in a decoder are, of necessity, small. Tubes and all other components must therefore be highly stable and reliable. Present-day type 5687 tubes are not good enough for this application. It is understood that Tung-Sol, the manufacturer of 5687 tubes, is trying to improve the reliability of these tubes. If future deliveries show no improvement in reliability, the multivibrators should be redesigned for other tubes, e.g., type 2C51. If such a change becomes necessary, it will not be possible to synchronize the multivibrators at frequencies greater

than 2 mc. With the exception of its poor reliability, the type 5687 tube is unquestionably the best tube available for this application. A change in tube type should therefore be made only if absolutely necessary.

3.62 Use of Other Devices

While the use of acoustic delay lines for DE 3 and DE 4 in this investigation would have led to excessive expense, it may be economical in practical applications to use mercury delay lines for DE 3 and DE 4. Modern mercury delay lines have a large number of signal channels. Two of these channels would be required for each conversion device, and if the total number of conversion devices is large enough to make full use of a mercury delay line, economical design may result. Recent experience with mercury delay lines shows that they will be fully satisfactory from the point of view of accuracy, reliability, and stability.

Attention has recently been called to the use of magnetic ferrites as delay elements.[1] At the present time, insufficient information is available to allow evaluation of the possibilities. Future work should consider the use of magnetic ferrites for DE 3 and DE 4, since the reliability of these materials is supposed to be excellent.

3.63 Checking

Finally, future development should consider the possibilities of incorporating a method of checking the decoder. The checking methods developed for the Whirlwind computer are not applicable to the decoder, which is an analog device. Of course, checking the decoder is just as important as checking the computer itself. New checking methods must therefore be developed.

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1. Ref. 34

4.0 TESTS USING THE COMBINED SYSTEMS

In order to get further information on the accuracy, reliability, and also the frequency response of the two systems developed in this thesis, it was decided to perform a test in which the coder fed the decoder directly. This, as we shall see, results in a considerable saving in the amount of test equipment needed.

We have shown in Section 2.31 that the coding equipment, which converts a shaft position into a binary number, generates a pair of pulses the time interval between which is proportional to the position of the shaft. Ordinarily, these pulses would actuate a flip-flop and counter arrangement to produce the binary pulse-coded number. In order to avoid the necessity of setting up a binary counter, the accuracy of this system was checked by actually counting pulses, as described in Section 2.51. This type of testing is necessarily static; yet it is desirable to test the system under dynamic conditions. When the coder and the decoder are combined, dynamic tests can be carried out with a minimum amount of additional equipment.

In Section 3.31, it is shown that the decoder, which converts a binary number to a voltage amplitude, actually carries out the conversion in two steps. The second of these steps involves the conversion of a pulse-position-modulated signal to a voltage amplitude and is carried out in the so-called conversion device. In order to test this unit, there must be available, on separate lines, two pulses, the interval between which is adjustable and is accurately known. The setup shown in Figure 33 will give

the necessary pair of pulses through the use of gate-and-delay units. This is sufficient for qualitative tests, but is difficult to use in quantitative measurements, since the time between the two pulses is not accurately known.

In order to eliminate test equipment and yet make it easy to perform dynamic tests, the two systems were combined so that the PPM signals from the coder fed the conversion device. The two connections that are made in order to combine the systems are indicated in Figures 14 and 26.

Before discussing the dynamic tests performed, let us first consider the dynamic characteristics of the systems. There are two frequency ranges of interest in these systems: information frequencies and sampling frequencies.

The information frequencies are those describing the motion of the shaft. Since this is a mechanical motion, the frequency components of the information range from 0 to 50 cps.

The sampling frequencies are introduced by the fact that new information is not supplied continuously, but only at discrete intervals. It is well known that if the sampling is not to introduce any distortion, the sampling frequency must be more than twice the highest frequency component of the information. Thus, if the highest frequency component were 50 cps, the sampling frequency would have to be somewhat higher than 100 cps. For more slowly moving shafts, the sampling frequency might be lower.

Both of these frequency ranges can be handled by the coder. Previous discussion has shown that the coder can furnish a new pair of output pulses for every cycle of the reference sinusoid. Since the frequency

of the reference sinusoid is 4 kc, we see that the coder can furnish new samples at the rate of 4 kc. The coding system is therefore capable of handling information frequencies up to nearly 2 kc. Since this frequency is many times higher than the frequency components described above, we can conclude that the coder will not introduce any frequency distortion.

The decoder is also capable of handling the required frequency components. In order to reach the output of the decoder, a pair of input pulses to the conversion device must travel through the delay elements at least once. The information pulse is delayed 4.5 microseconds in DE 2 and 140 microseconds in DE 4. The total delay is thus 144.5 microseconds. Hence the decoder can accept information at a maximum rate of $1/144.5 \times 10^{-6}$, or nearly 7 kc. Up to the integrator, therefore, more than sufficient bandwidth is available.

The purpose of the integrator is to extract the information from the gate-width-modulated signal produced by the decoder. In terms of frequency components, the integrator is a low-pass filter which, ideally, passes all of the information frequencies and none above. A non-ideal filter may (1) attenuate some of the higher frequency components of the information, and (2) pass some of the unwanted components introduced by the sampling process. Thus the filter is the only possible source of frequency distortion of the information, and the frequency response of the system over the range from 0 to 50 cps should be identical with the frequency response of the filter used in the integrator. Any deviations from this would indicate that the equipment was not operating properly.

A frequency-response test was made in the following manner: The shaft of the control transformer connected to the coding system was caused to oscillate in a sinusoidal manner by means of a mechanical setup. The frequency of oscillations could be varied from 1 to 50 cps. The coding system was connected to the decoding system as described above, and the blocking oscillator of Figure 14 was set so that it produced a pulse about 50 times per second. This is the sampling frequency.

The filter in the integrator consisted of an 18,000 ohm resistor in parallel with a 1.0 microfarad condenser. It will be seen that this R-C network is a very rough approximation to an ideal low-pass filter. (In practical applications, the design of the filter will be governed by over-all system requirements.) The half-power point of the R-C network is at approximately 9 cps. It was chosen to be this low so that the effects of the filter network would be noticed at frequencies much lower than those at which the effects of sampling would be noticed. The amplitude and phase of the output of the integrator were measured as a function of frequency. The results of this test indicated that the amplitude of the integrator output fell off with increasing information frequency in exactly the same way that the calculated impedance of the R-C network does. Also, the phase shift introduced was the same as that of the R-C network, except for an added phase shift due to the oscilloscope amplifier used in the test setup. In other words, the frequency response of the combined systems is determined entirely by the filter used in the integrator, provided that the sampling frequency is more than twice the highest frequency component of the information handled.

Finally, in order to demonstrate that the combined systems operate properly under dynamic conditions as well as statically, the pictures in Figure 35 were taken. The condenser in the integrator was changed to 0.1 microfarad. This new filter does not remove the sampling frequency, which was 100 cps in this case. Thus we see in the pictures the effects of sampling, which causes the sinewave to be approximated by a series of step functions. The pictures also illustrate the holding action of the decoder. Note that in the intervals between new samples the output is nearly constant.

The last picture in Figure 35 shows the output of the integrator superimposed upon the output of an additional synchro attached to the drive shaft. This synchro has a stator voltage at a frequency of 1000 cps. The output of the rotor of the additional synchro is the 1000 cps signal modulated by the position of the shaft. The modulation envelope is, therefore, identical with the input to the coding setup. Note how the output follows the input as closely as the sampling will allow.

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LIST OF FIGURES

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1	A 34656	Binary Counter
2	A 45040	System for Converting PPM Signals into Binary Pulse-Coded Numbers
3	A 45043	Simplified Block Diagram of the System for Converting Shaft Position to a Binary Pulse-Coded Number
4	A 45045	Timing Relationships of Various Waveforms
5	A 45042	Block Diagram of System Used for Converting Shaft Position to Pulse Interval
6	A 45029	Waveforms
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17	A 45051	Error in Angular Position as a Function of the Number of Pulses.
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19	A 45050	Error Curve with Two Control Transformer System
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34	A 45057	Error in Integrator Output as a Function of Time Interval between Control & Information Pulses Supplied to Decoder

Figure Number	Drawing Number	Title
35	A 48061	Waveforms
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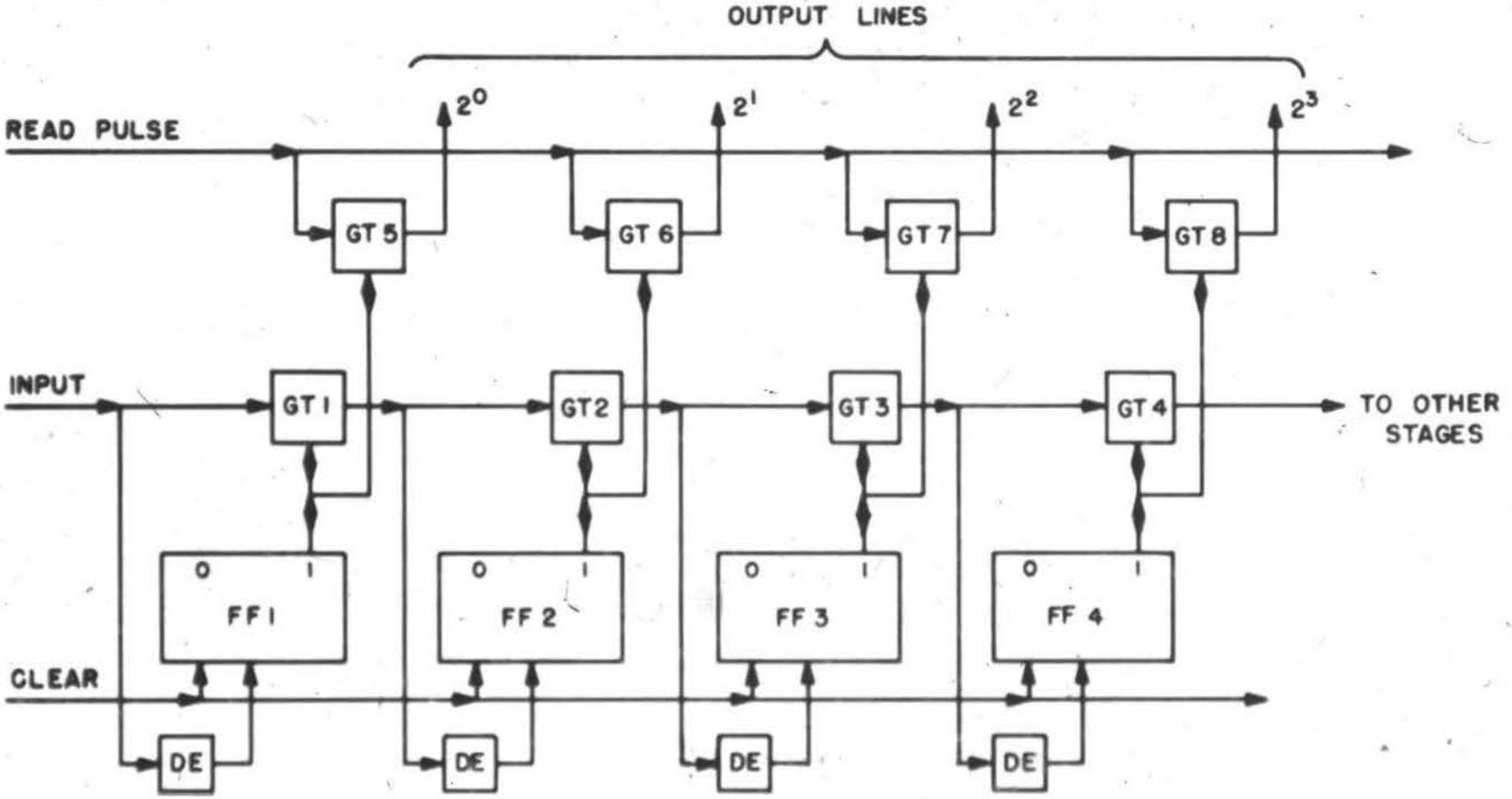
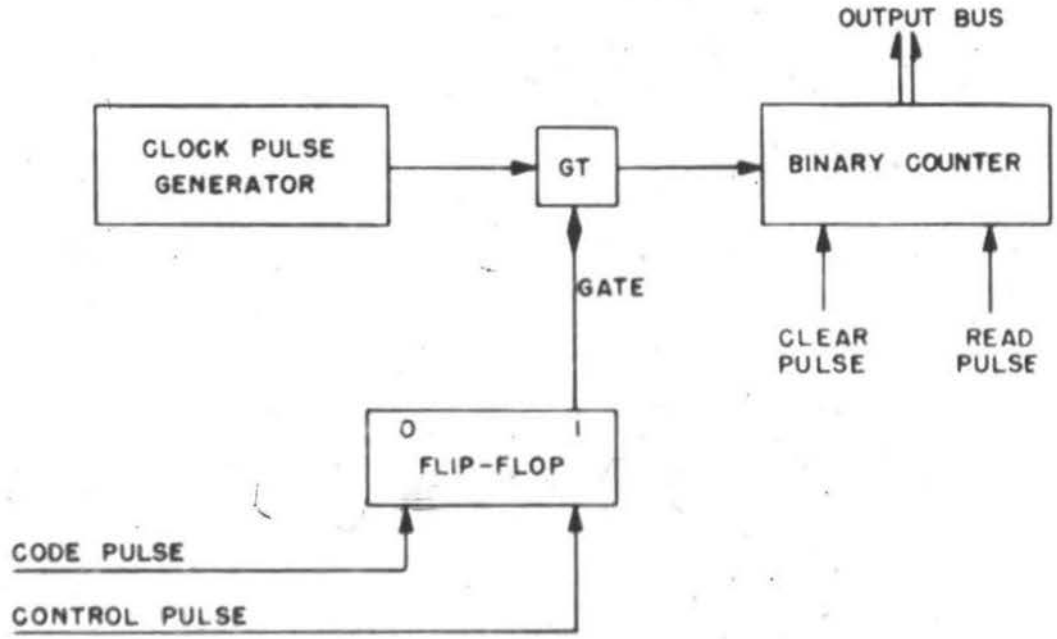
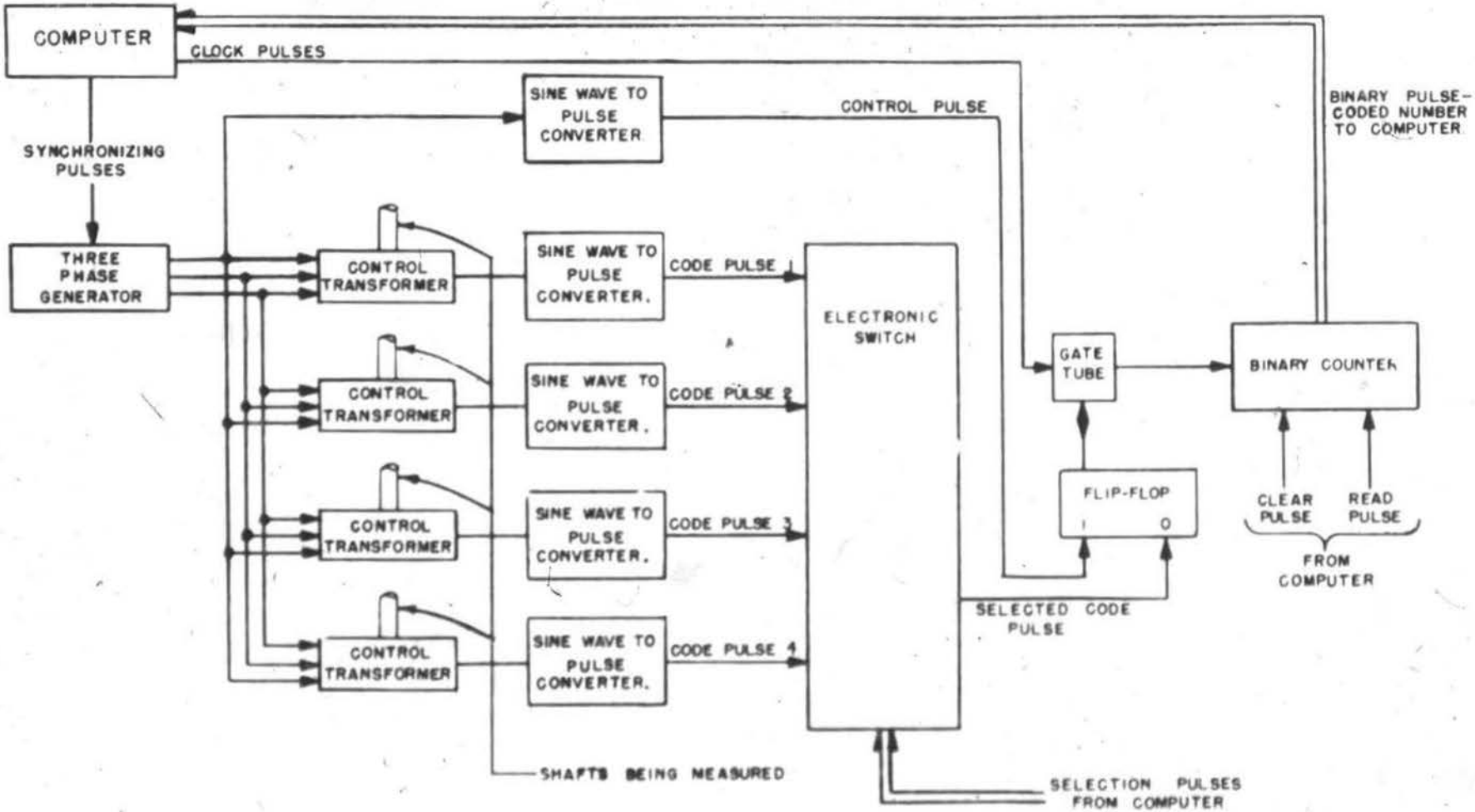


TYPICAL BINARY COUNTER WITH PROVISION FOR READING OUT



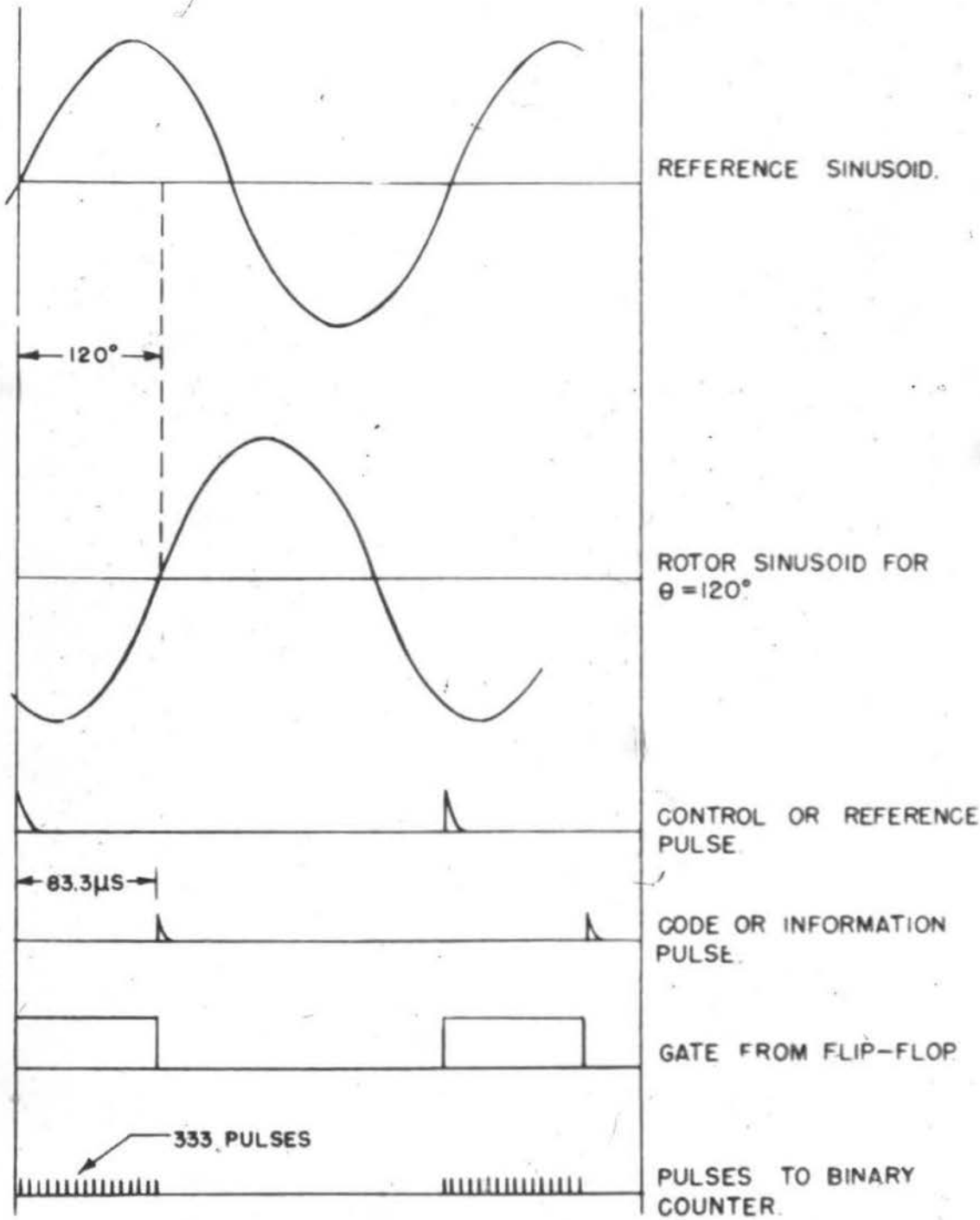
SYSTEM FOR CONVERTING PULSE-POSITION-MODULATED SIGNALS INTO BINARY PULSE-CODED NUMBERS.

FIG. 2



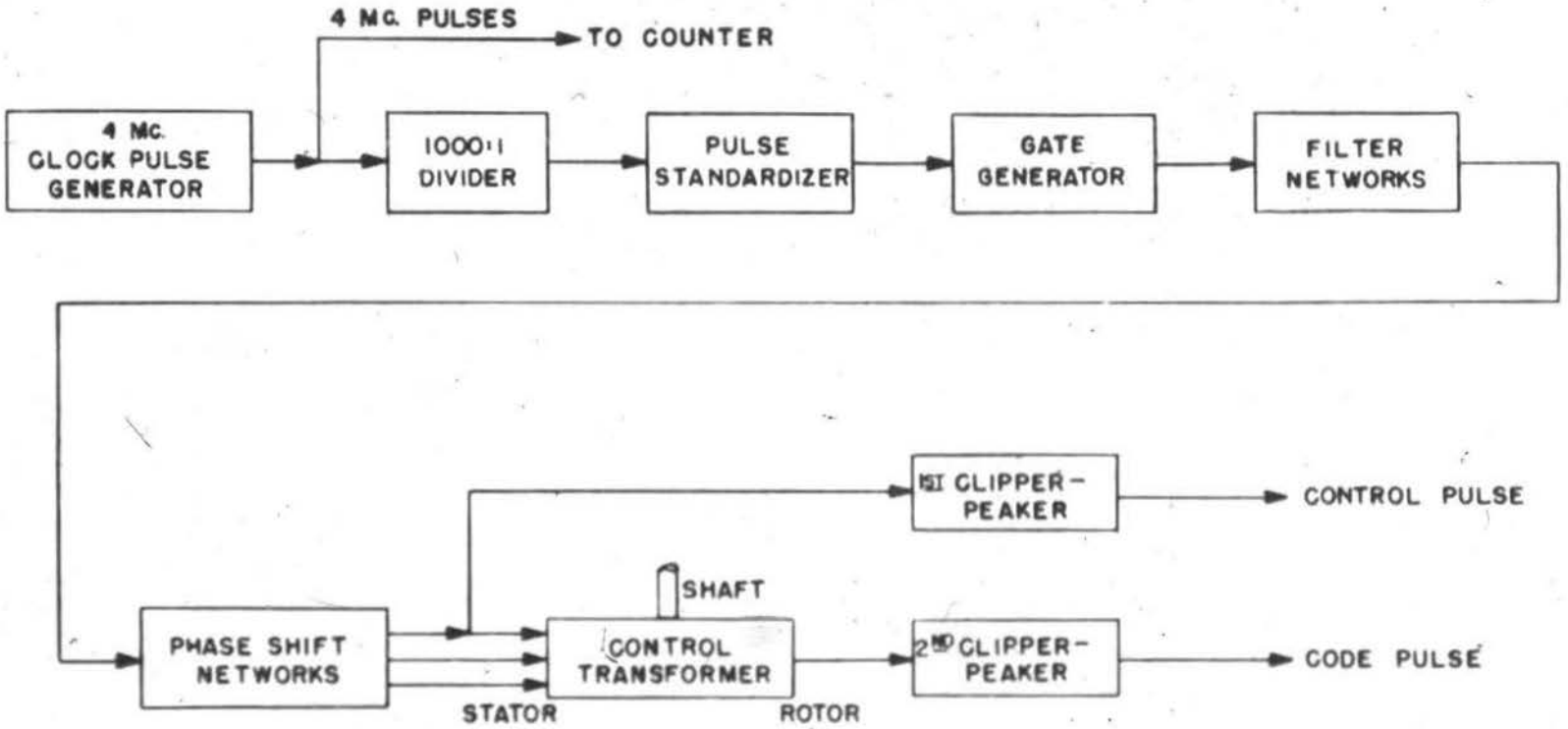
SIMPLIFIED BLOCK DIAGRAM OF THE SYSTEM FOR CONVERTING SHAFT POSITION TO A BINARY PULSE-CODED NUMBER.

FIG. 3



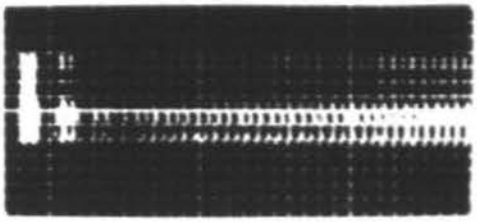
TIME RELATIONSHIPS OF VARIOUS WAVEFORMS

FIG. 4

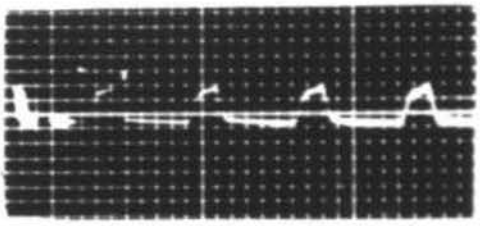


BLOCK DIAGRAM OF THE SYSTEM USED FOR CONVERTING SHAFT POSITION TO PULSE INTERVAL.

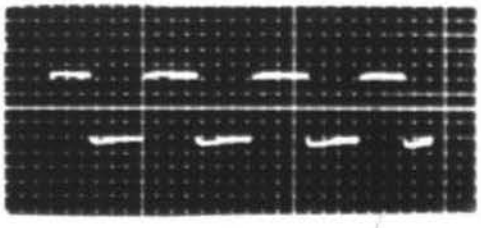
FIG. 5



A. 4 M_c CLOCK PULSES



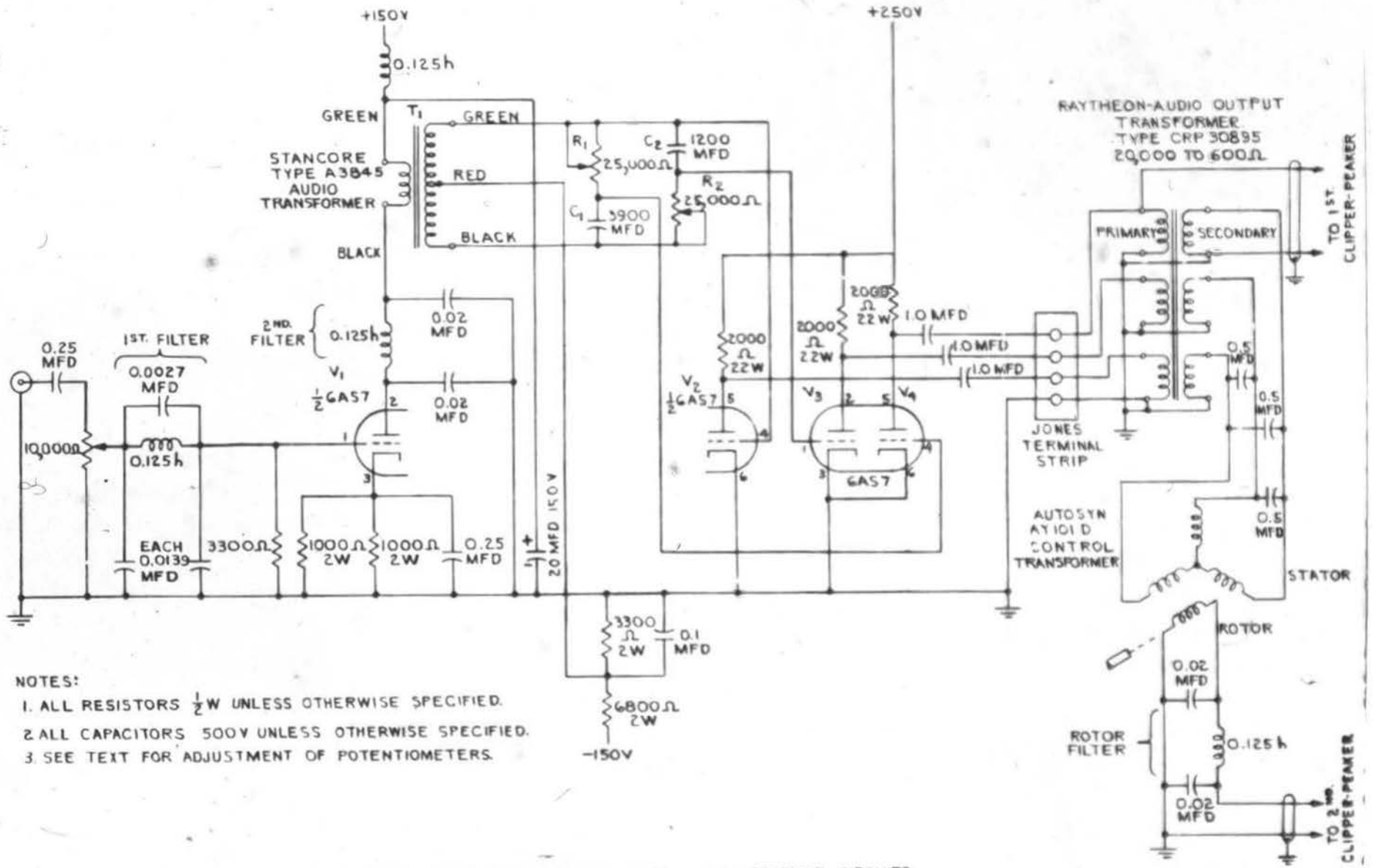
B. OUTPUT OF 10/1 DIVIDER



C. OUTPUT OF GATE GENERATOR

A-45029

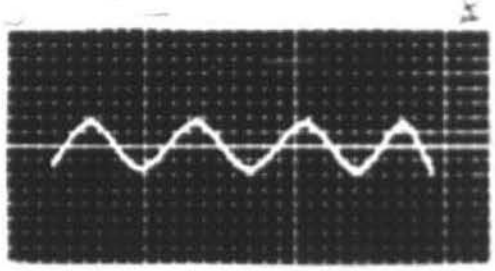
FIG. 6



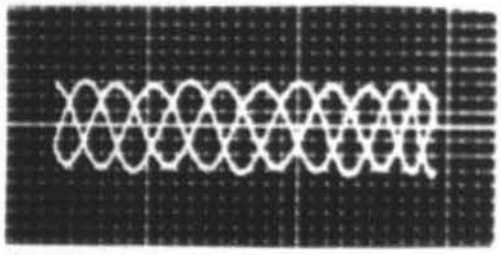
NOTES:

1. ALL RESISTORS ½W UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS 500V UNLESS OTHERWISE SPECIFIED.
3. SEE TEXT FOR ADJUSTMENT OF POTENTIOMETERS.

FILTER, PHASE SHIFT NETWORK, AND CONTROL TRANSFORMER CIRCUITS.



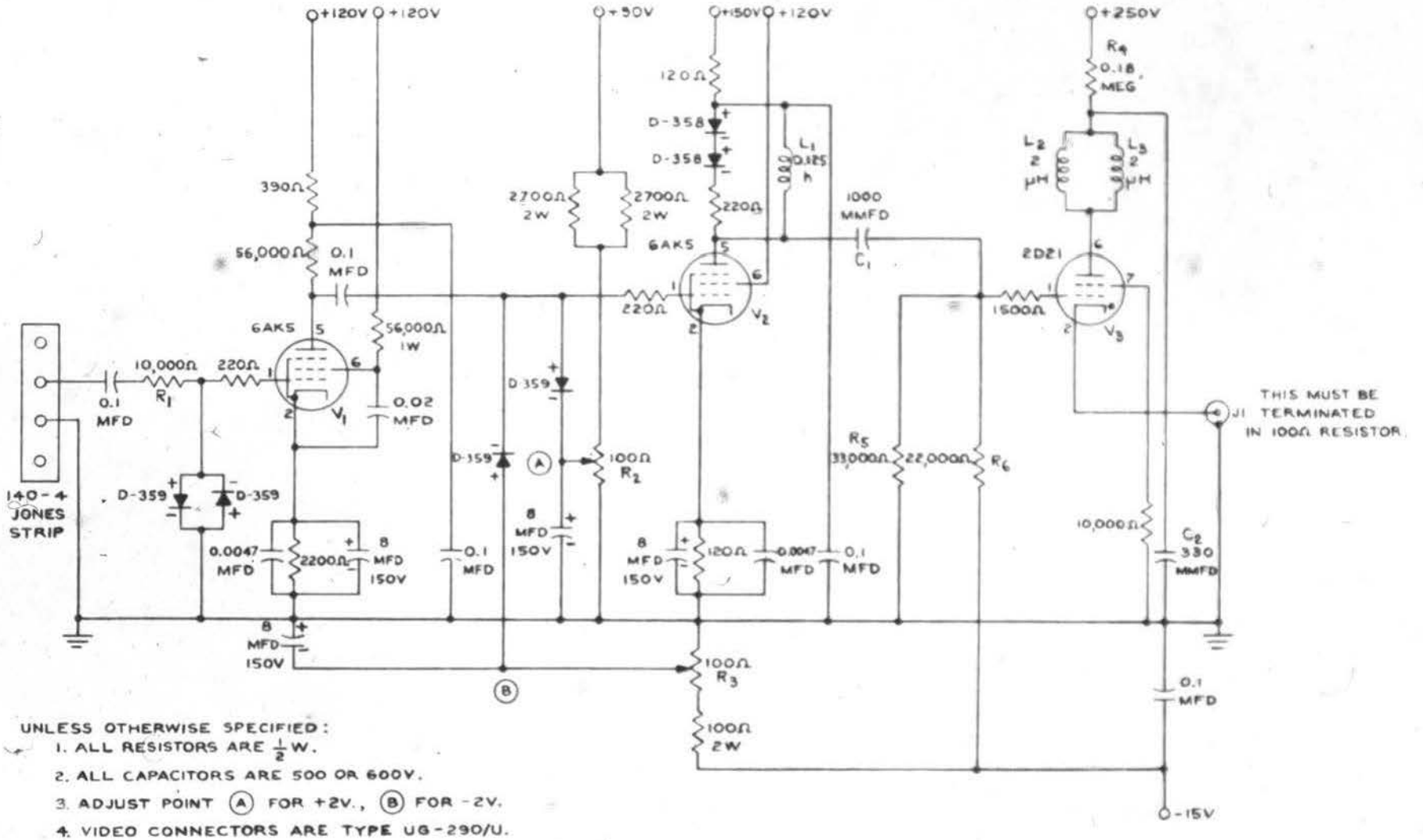
A. SIGNAL AFTER 1ST FILTER



B. THE 3 PHASE VOLTAGES

A-45030

FIG. 8

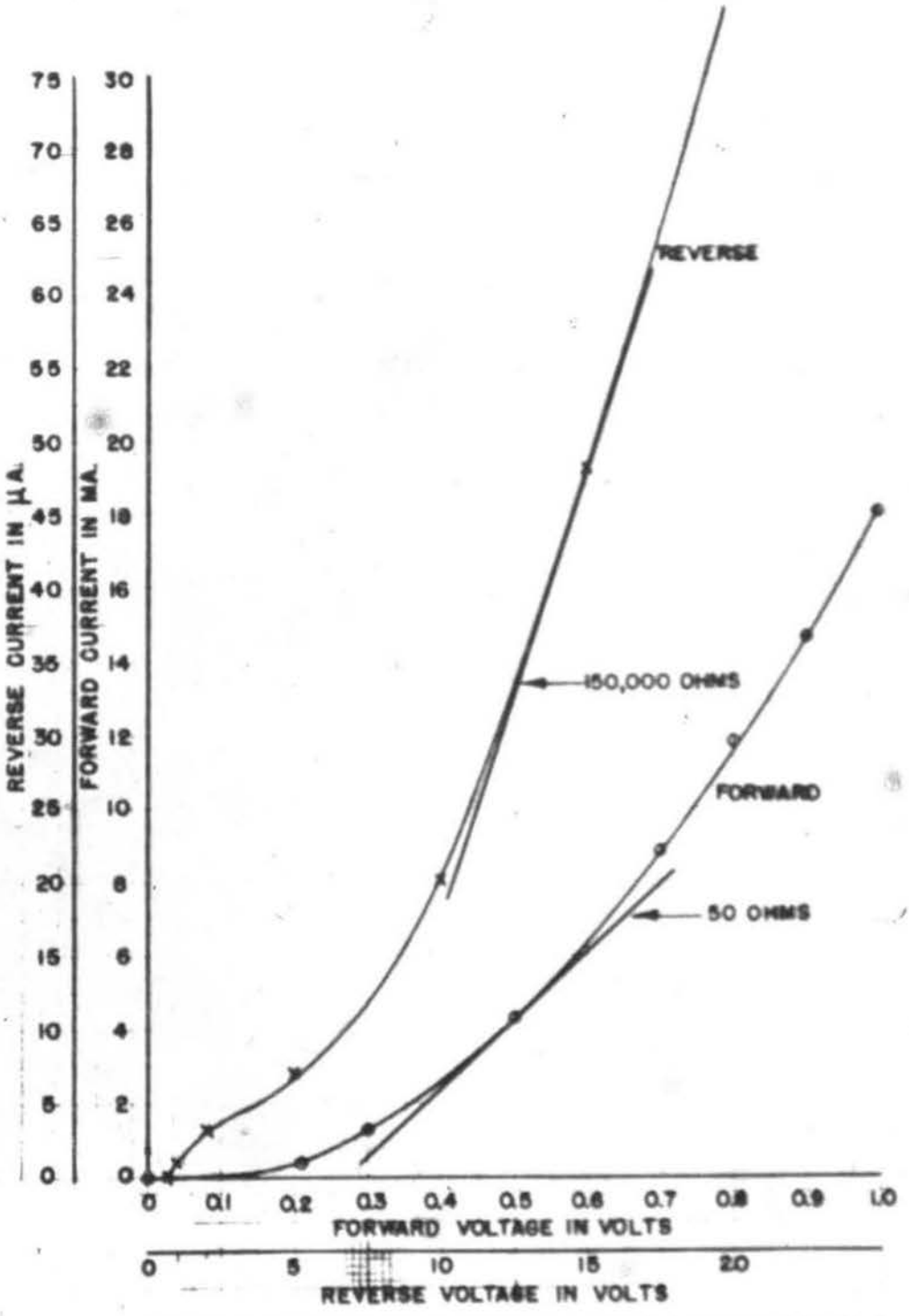


UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE $\frac{1}{2}$ W.
2. ALL CAPACITORS ARE 500 OR 600V.
3. ADJUST POINT (A) FOR +2V., (B) FOR -2V.
4. VIDEO CONNECTORS ARE TYPE UG-290/U.

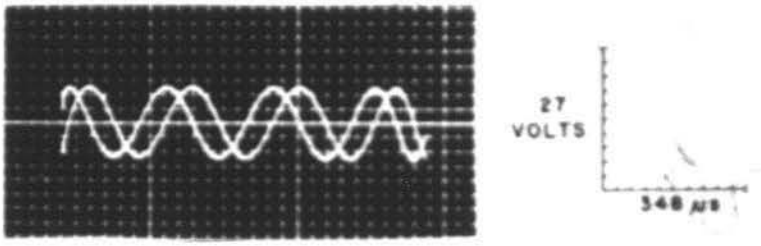
CLIPPER-PEAKER

FIG. 9

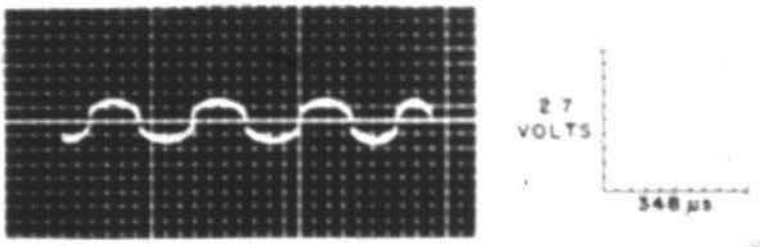


STATIC CHARACTERISTICS OF A D-359 CRYSTAL.

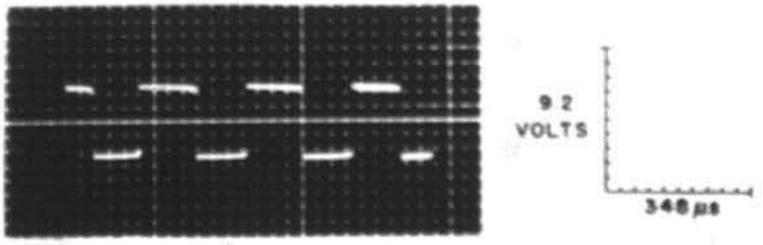
FIG. 10



A. ROTOR SINUSOID FOR
θ=0° AND θ=90°



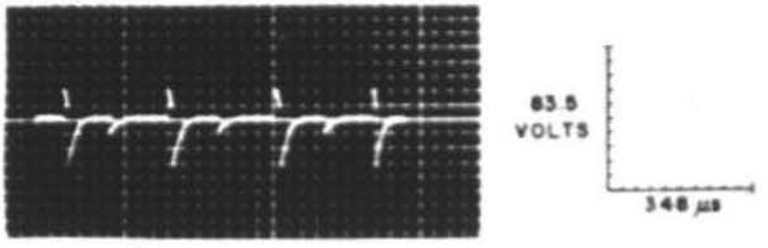
B. VOLTAGE ACROSS FIRST CLIPPER DIODES
IN CLIPPER-PEAKER



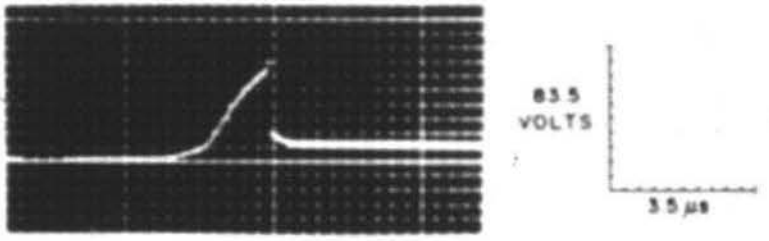
C. OUTPUT OF 1ST STAGE IN
CLIPPER-PEAKER

A-45033

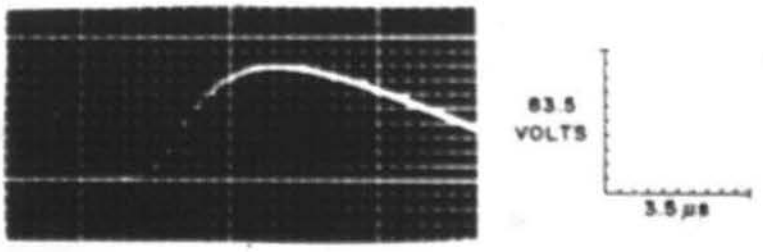
FIG. 11



A. PLATE WAVEFORM - 2ND STAGE
IN CLIPPER-PEAKER



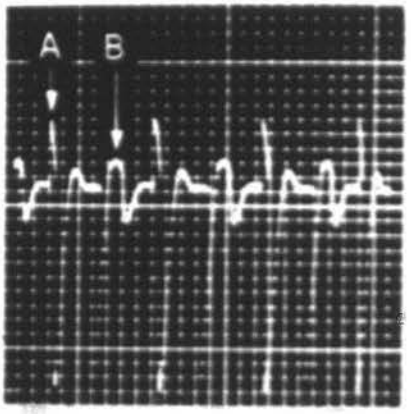
B. PEAKER GRID WAVEFORM JUST
BEFORE THE PEAKER FIRES

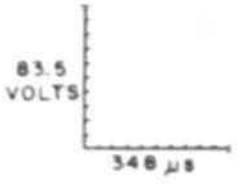


C. PEAKER GRID WAVEFORM WITH
THE PEAKER TUBE REMOVED

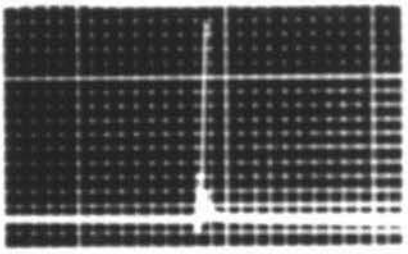
A-45034

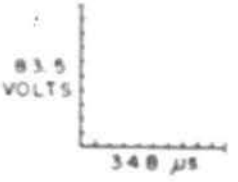
FIG. 12



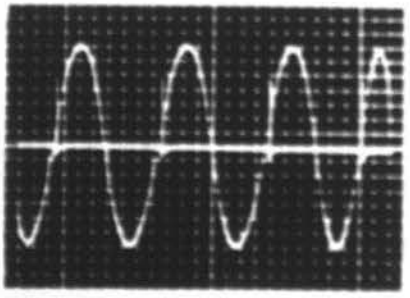


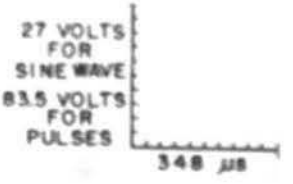
A. PEAKER GRID WAVEFORM WITH DAMPING CRYSTALS REMOVED FROM THE PLATE CIRCUIT OF THE SECOND STAGE.





B. OUTPUT OF PEAKER

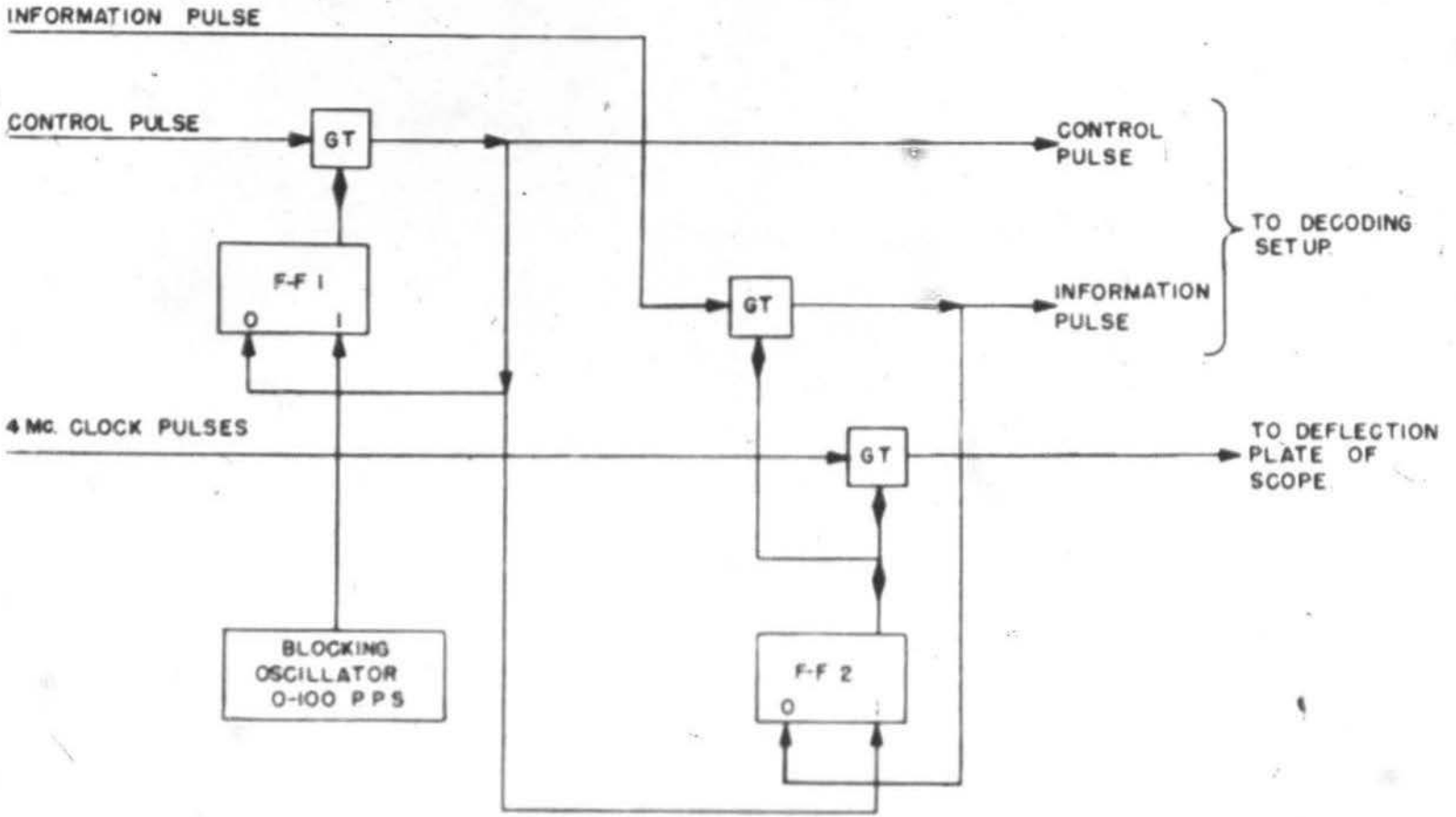




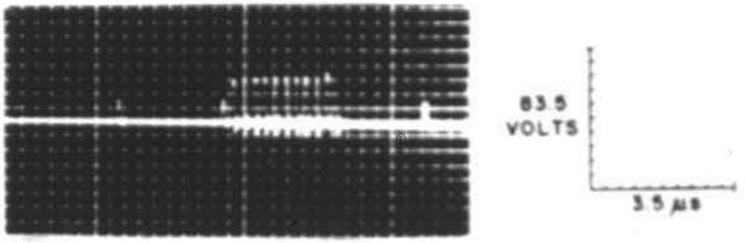
C. THE INPUT AND OUTPUT OF THE CLIPPER-PEAKER CIRCUIT SHOWN SIMULTANEOUSLY.

A-45035

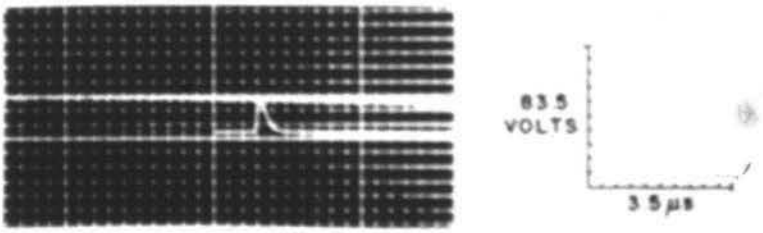
FIG. 13



BLOCK DIAGRAM OF TEST SETUP



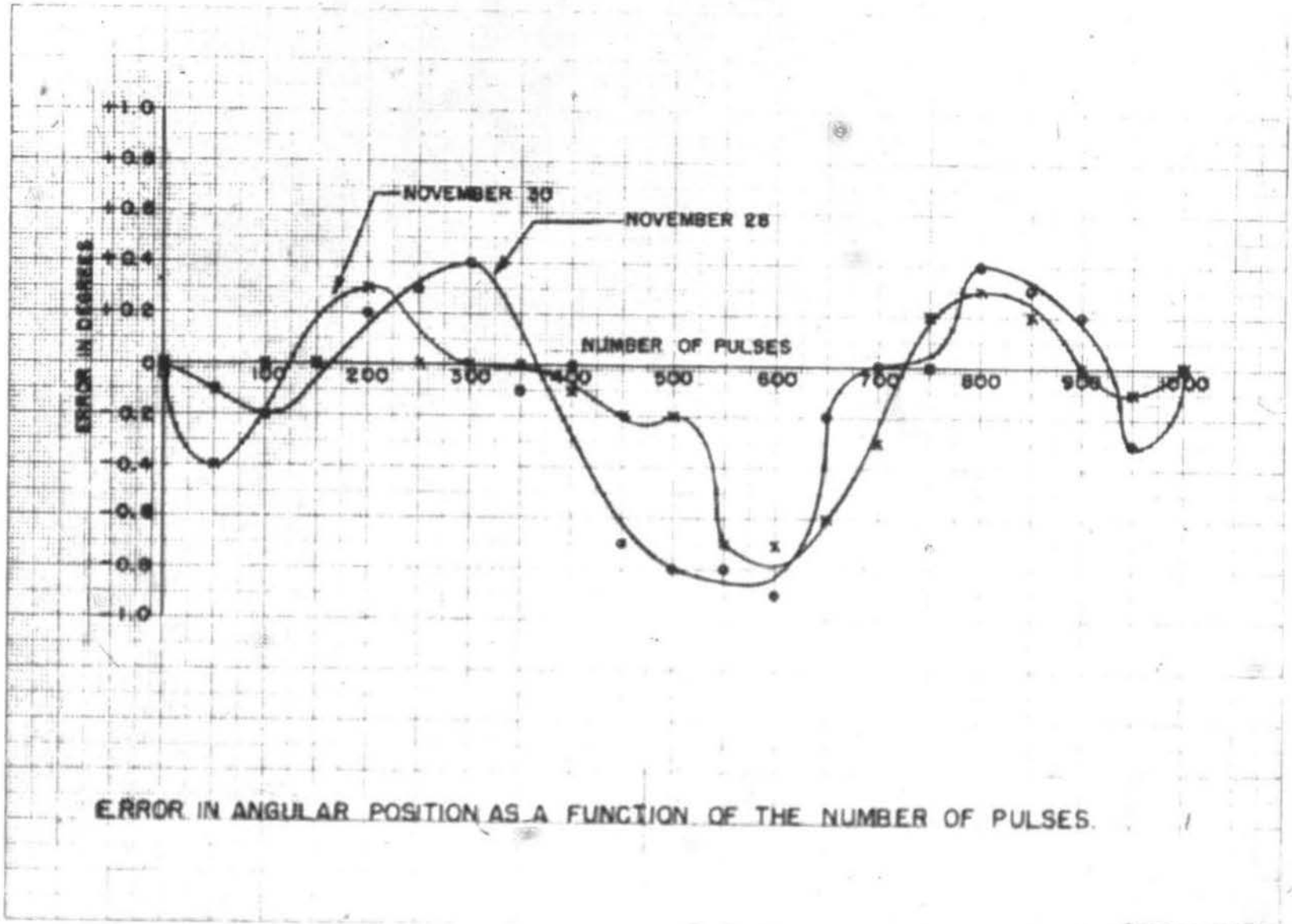
A. OUTPUT OF TEST SETUP SHOWING A COUNT OF 10 (EQUIVALENT TO 3.6°)



B. GATE FROM FF2 FOR θ = 0
NOTE OVERLAP OF BEGINNING AND END OF GATE

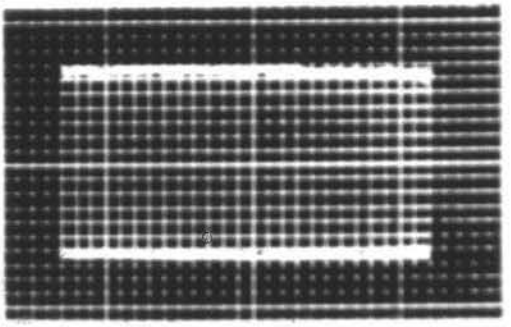
A-45031

FIG. 15

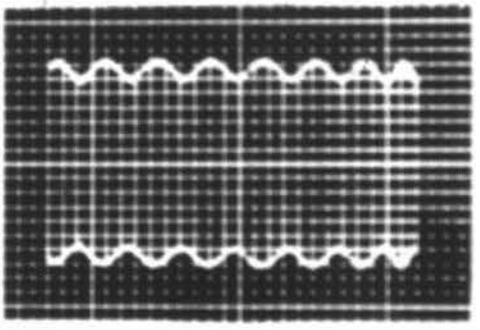


ERROR IN ANGULAR POSITION AS A FUNCTION OF THE NUMBER OF PULSES.

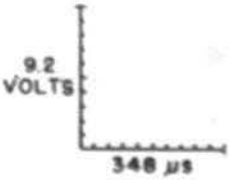
FIG 17



a SPINNING ROTOR OUTPUT
(PROPER PHASE ADJUSTMENTS)

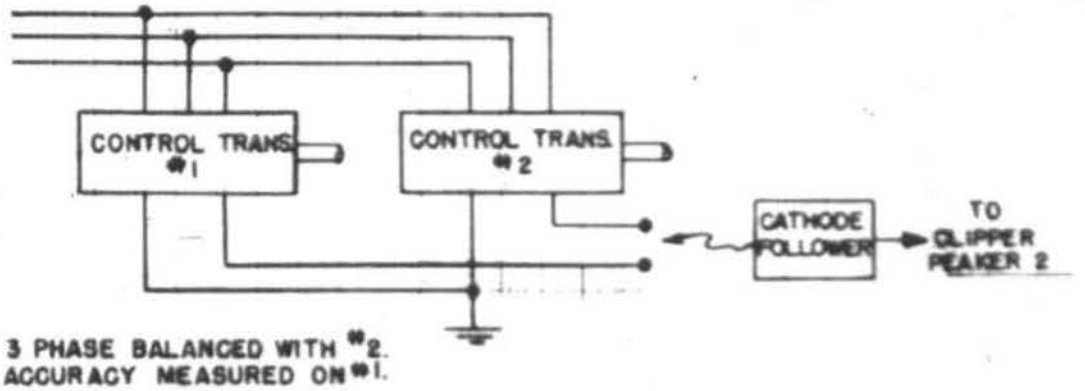


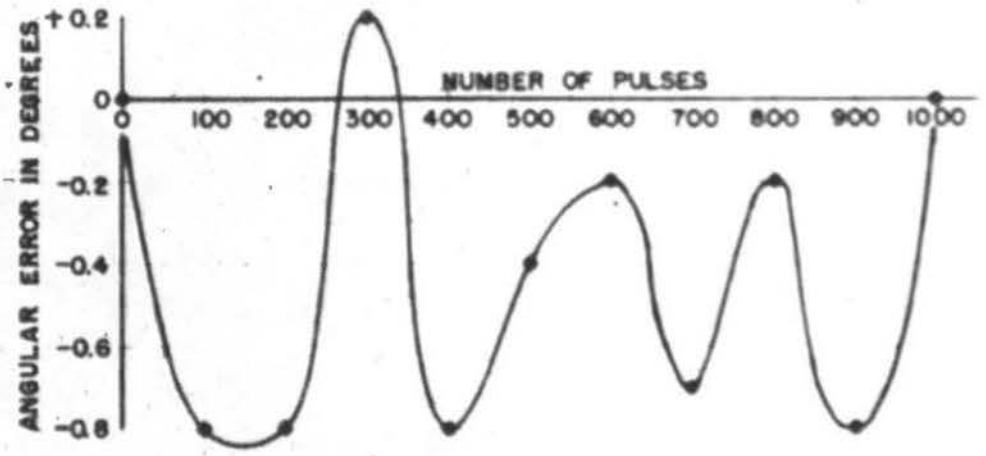
b SPINNING ROTOR OUTPUT
(IMPROPER PHASE ADJUSTMENTS)



A-45032

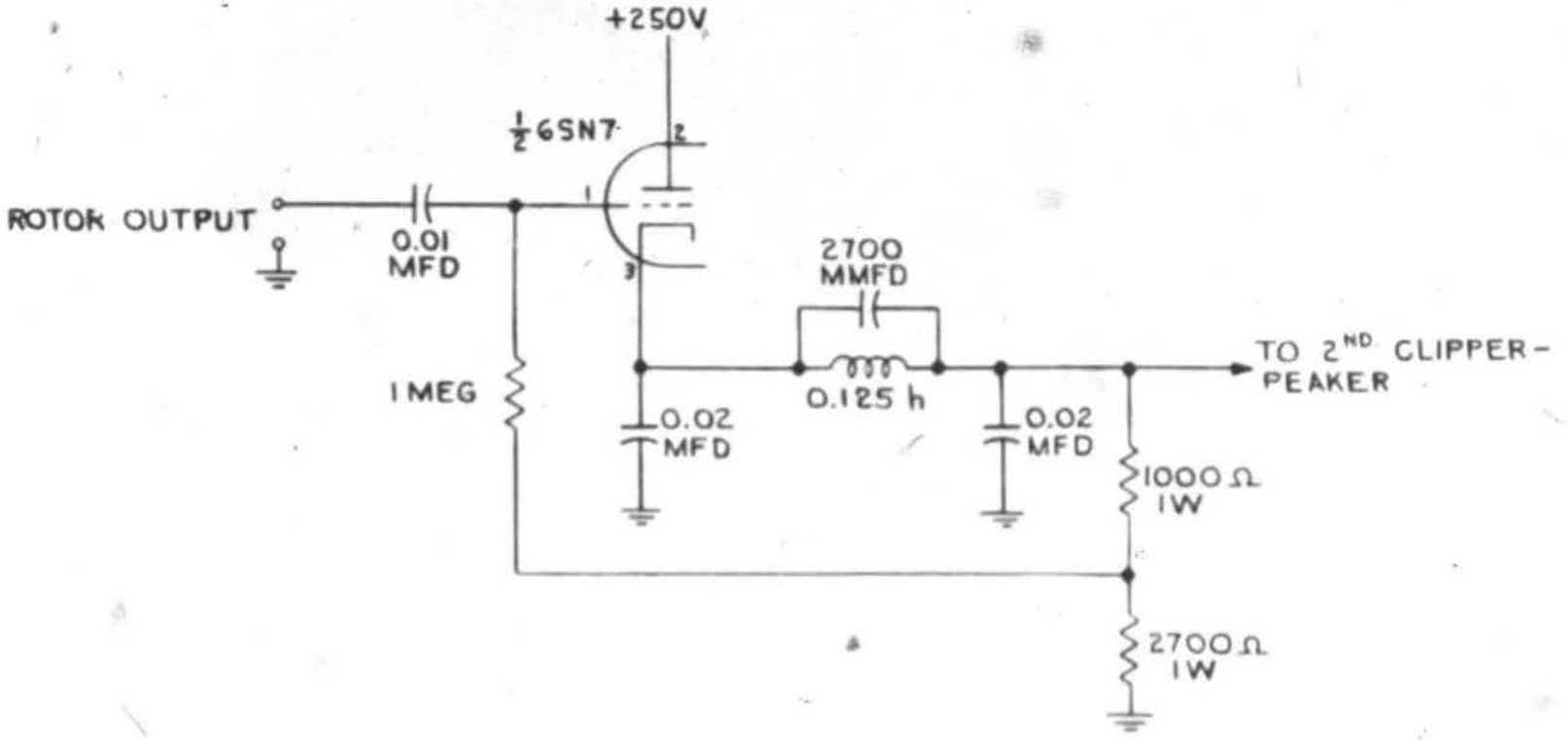
FIG. 18





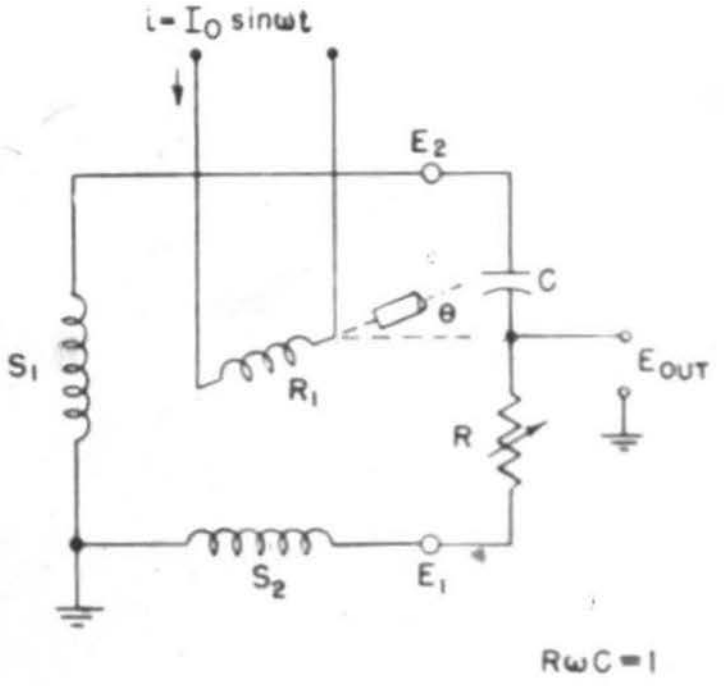
ERROR CURVE WITH TWO CONTROL TRANSFORMER SYSTEM

FIG. 19



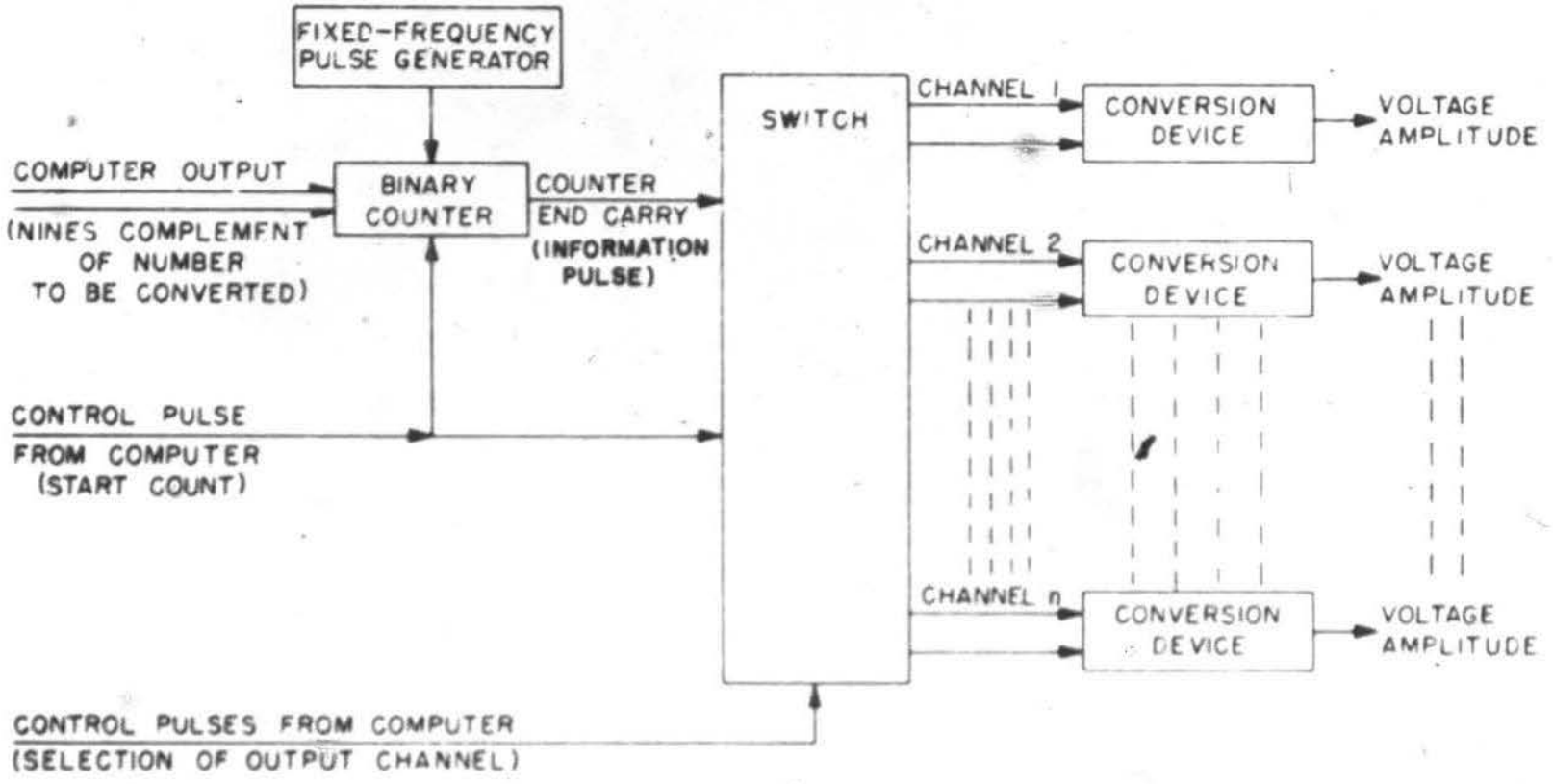
CATHODE FOLLOWER

FIG 20



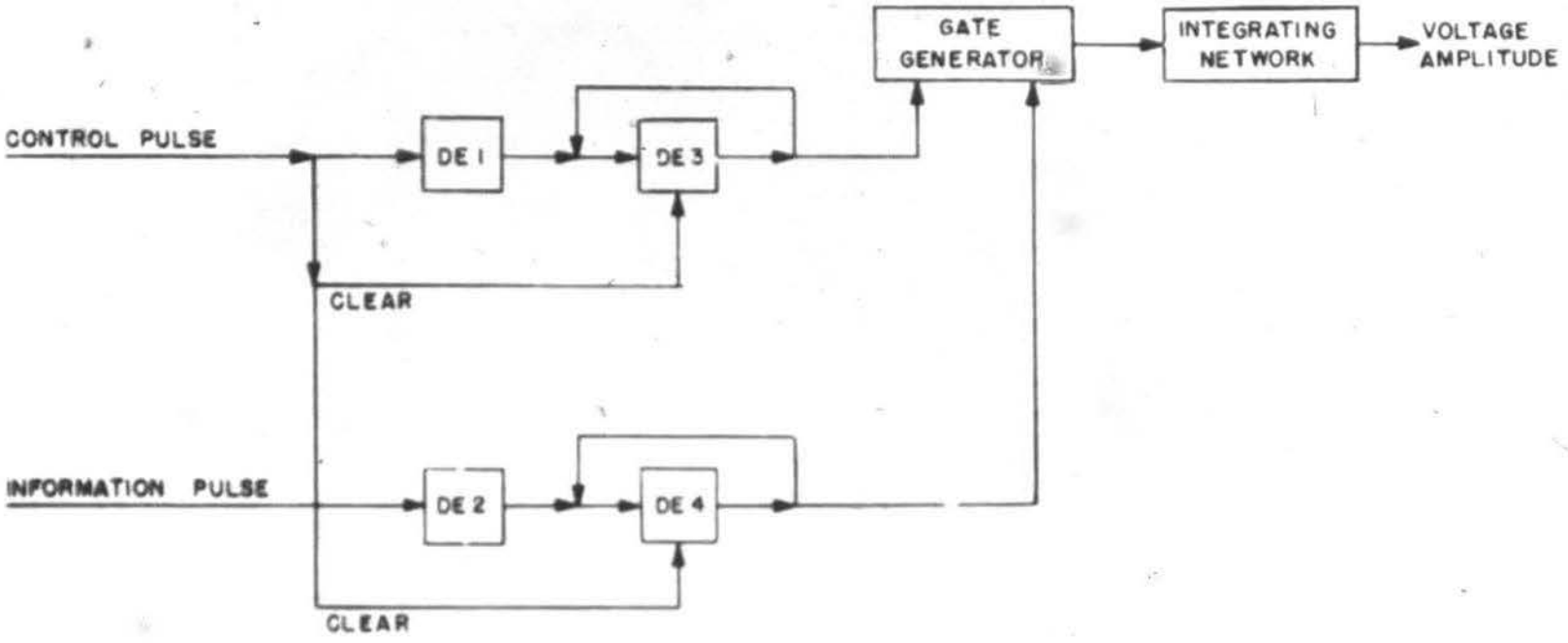
RESOLVER METHOD OF PHASE MODULATION

FIG. 21



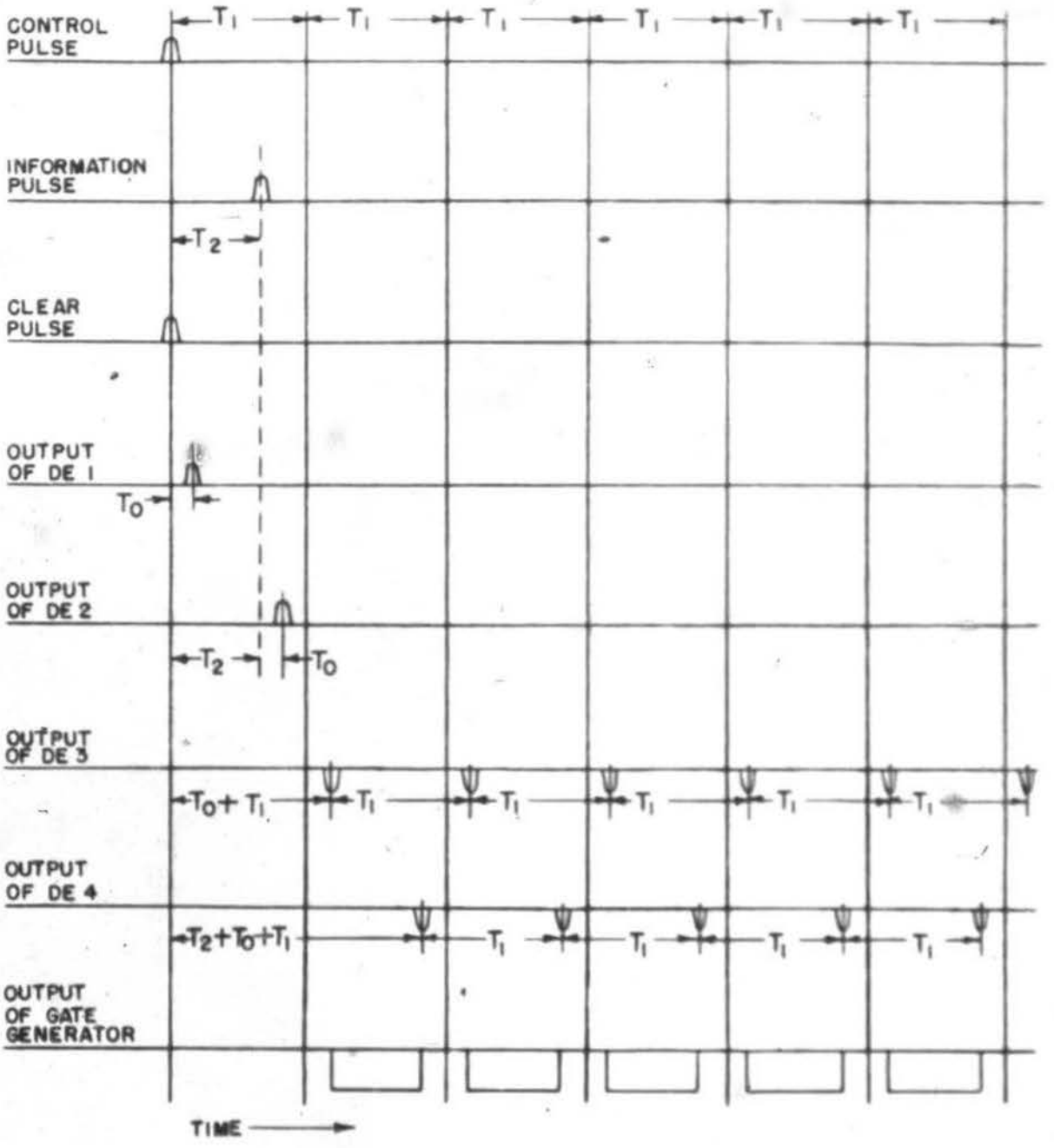
CONVERSION OF BINARY NUMBERS INTO VOLTAGE AMPLITUDES

FIG. 23



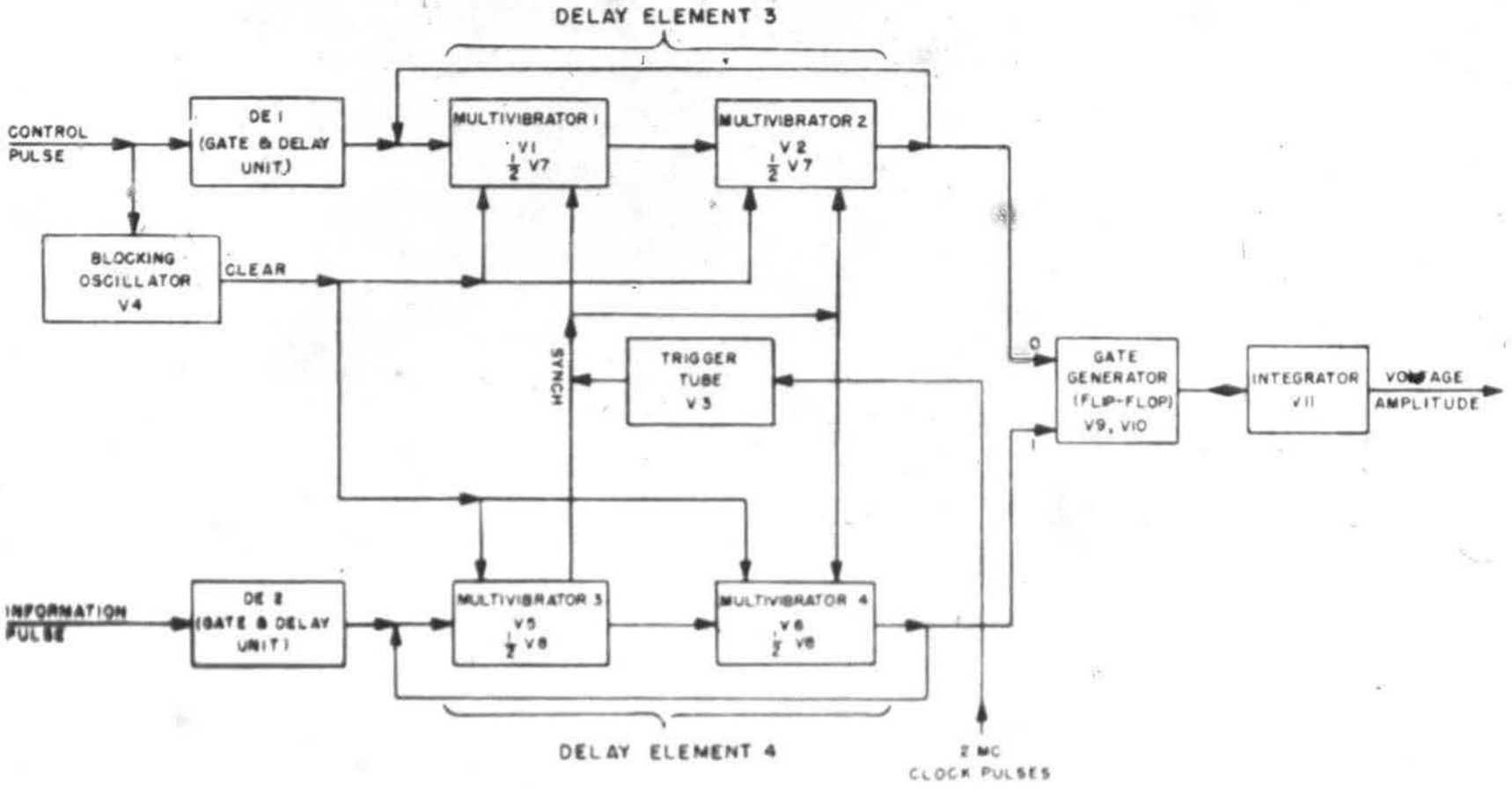
BLOCK DIAGRAM OF CONVERSION DEVICE.
(PAIR OF PULSES TO VOLTAGE AMPLITUDE)

FIG. 24



TIME RELATIONSHIP OF PULSES IN THE CONVERSION DEVICE
(PAIR OF PULSES TO SERIES OF GATES)

FIG.



BLOCK SCHEMATIC OF CONVERSION DEVICE
(PAIR OF PULSES TO VOLTAGE AMPLITUDE)

FIG. 26

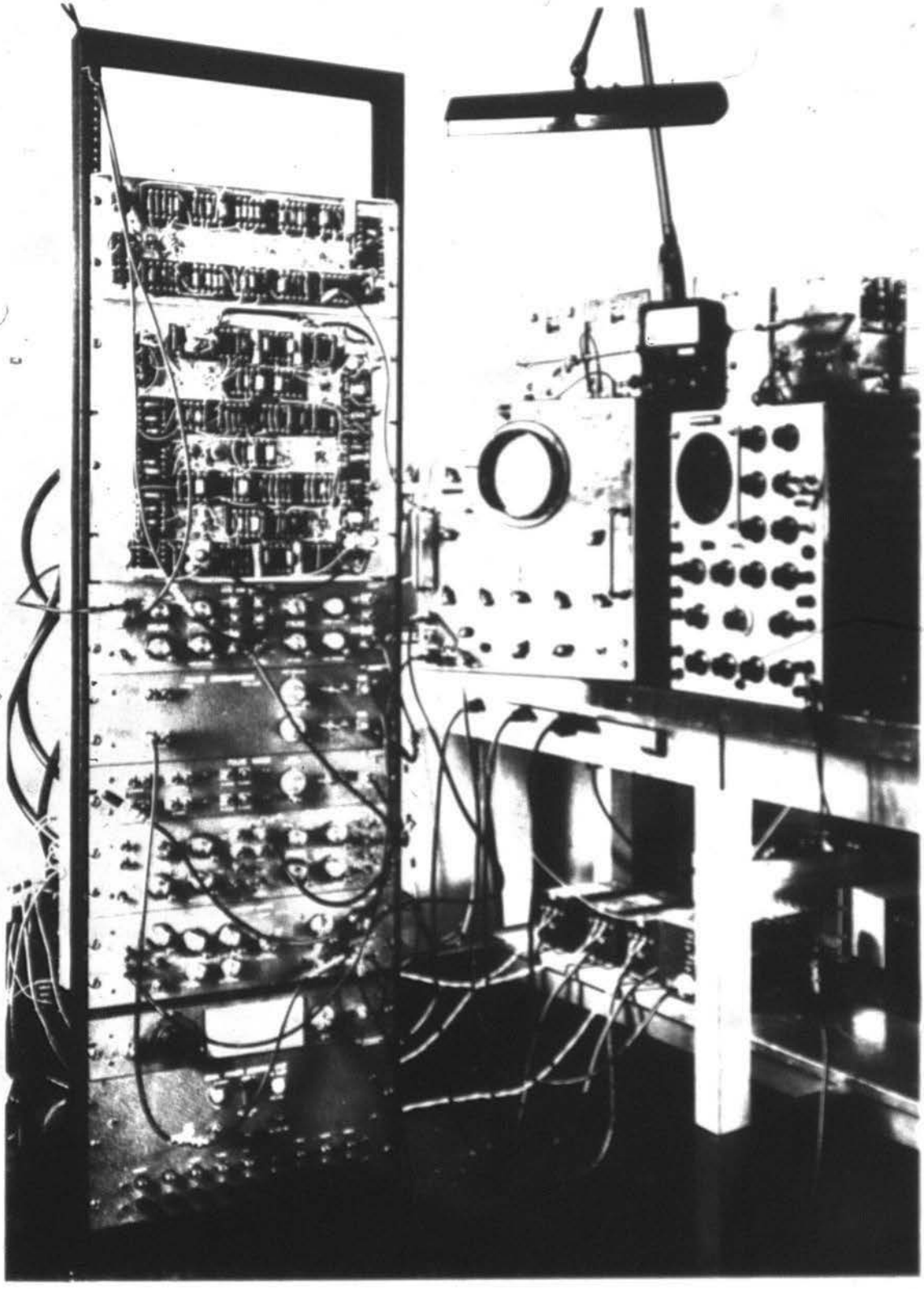


FIG. 27

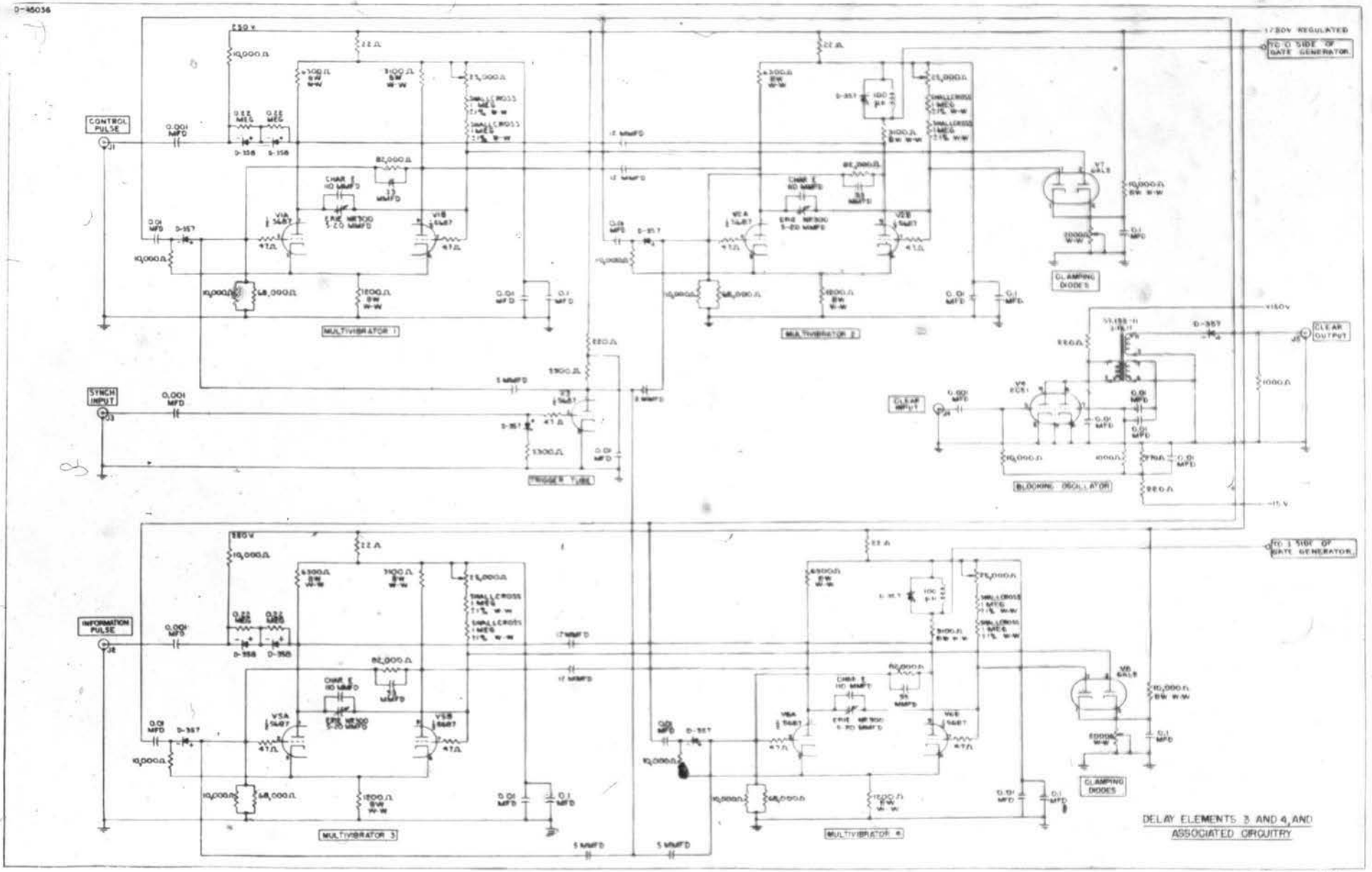
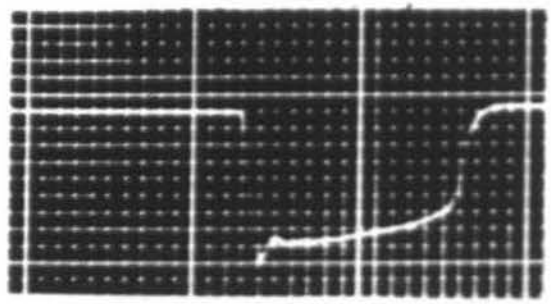
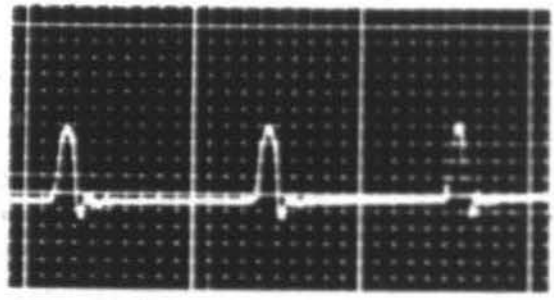

D-45036
CONTROL PULSE
SYNCH INPUT
INFORMATION PULSE
MULTIVIBRATOR 1
MULTIVIBRATOR 2
MULTIVIBRATOR 3
MULTIVIBRATOR 4
TRIGGER TUBE
BLOCKING OSCILLATOR
CLAMPING DIODES
CLAMPING DIODES
CLEAR INPUT
CLEAR OUTPUT
+150V REGULATED
TO C SIDE OF GATE GENERATOR
TO I SIDE OF GATE GENERATOR
-150 V
DELAY ELEMENTS 3 AND 4 AND ASSOCIATED CIRCUITRY

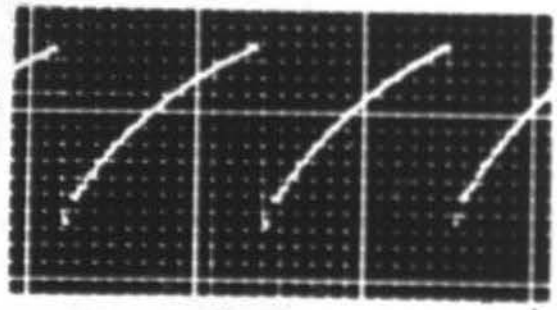
FIG. 28



(a) CLEAR-PULSE OUTPUT OF BLOCKING OSCILLATOR.
(SWEEP SPEED 0.85 μ SEC. / INCH)



(b) SYNCHRONIZING PULSE INPUT TO TRIGGER TUBE
(SWEEP SPEED 0.41 μ SEC. / INCH)

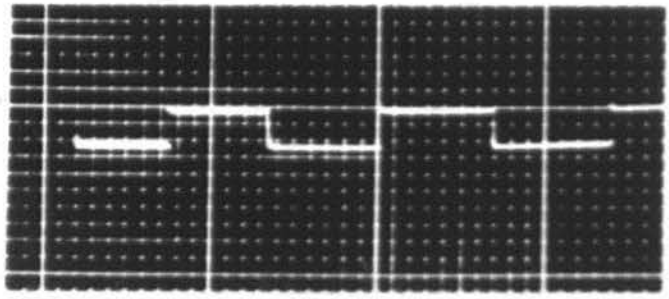


(c) SYNCHRONIZING PULSE OUTPUT FROM TRIGGER TUBE
(SWEEP SPEED 0.41 U SEC. / INCH)

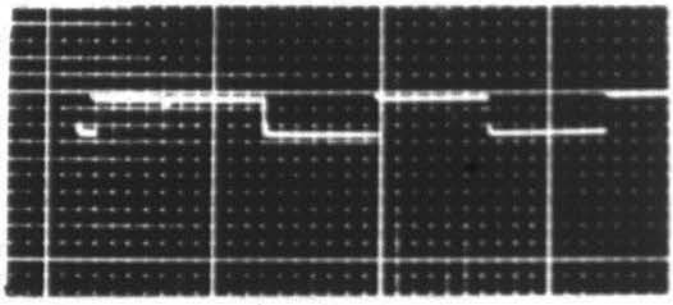
DEFLECTION SENSITIVITY: 60 VOLTS/INCH ON ALL PICTURES

A-45058

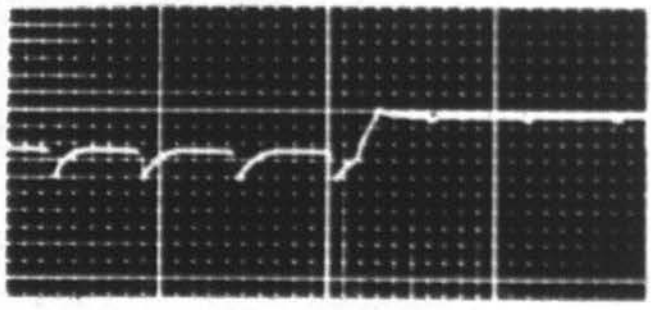
FIG. 29



(a) WAVEFORM AT CATHODES
OF MULTIVIBRATOR TUBES
(SWEEP SPEED 110 μ SEC. / INCH)



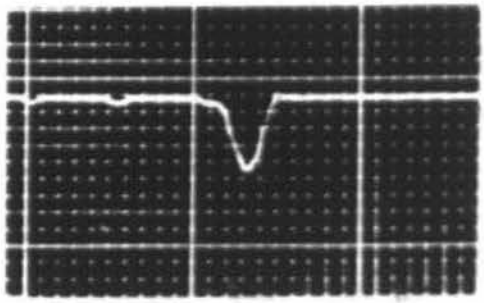
(b) EFFECT OF CLEARING ON WAVEFORMS
AT CATHODES OF TUBES IN MULTIVIBRATOR
(SWEEP SPEED 110 μ SEC. / INCH)



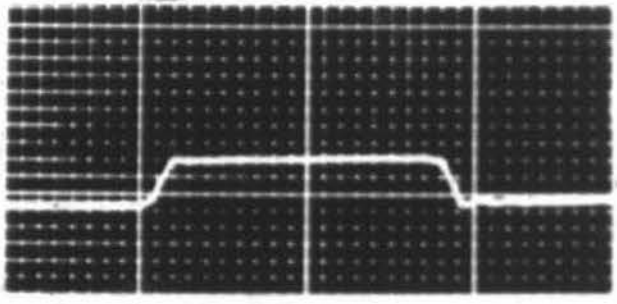
(c) EFFECT OF SYNCHRONIZATION ON WAVEFORMS
AT CATHODES OF MULTIVIBRATOR TUBES
(SWEEP SPEED 0.85 μ SEC. / INCH)

DEFLECTION SENSITIVITY: 60 VOLTS/INCH ON ALL PICTURES

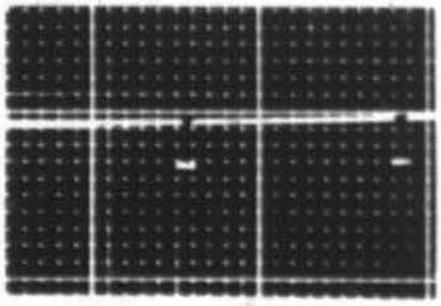
FIG. 30



(a) TRIGGER–PULSE OUTPUT
OF MULTIVIBRATORS 2 AND 4
(SWEEP SPEED 0.85 μ SEC / INCH)



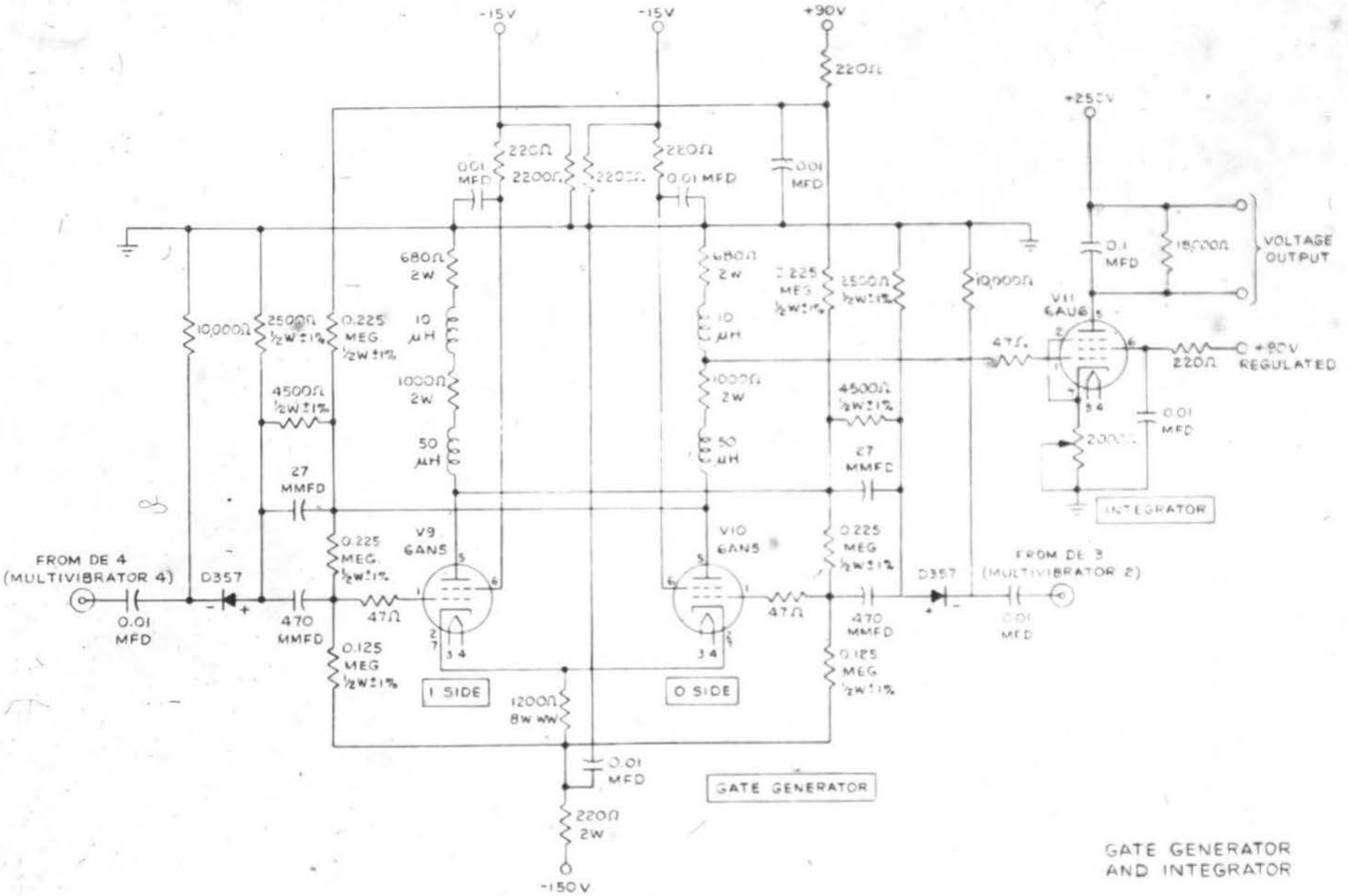
(b) OUTPUT OF GATE GENERATOR
CORRESPONDING TO NUMBER 0
(SWEEP SPEED 0.85 μ SEC./INCH)



(c) OUTPUT OF GATE GENERATOR
CORRESPONDING TO NUMBER 255.
(SWEEP SPEED 110 μ SEC. / INCH)

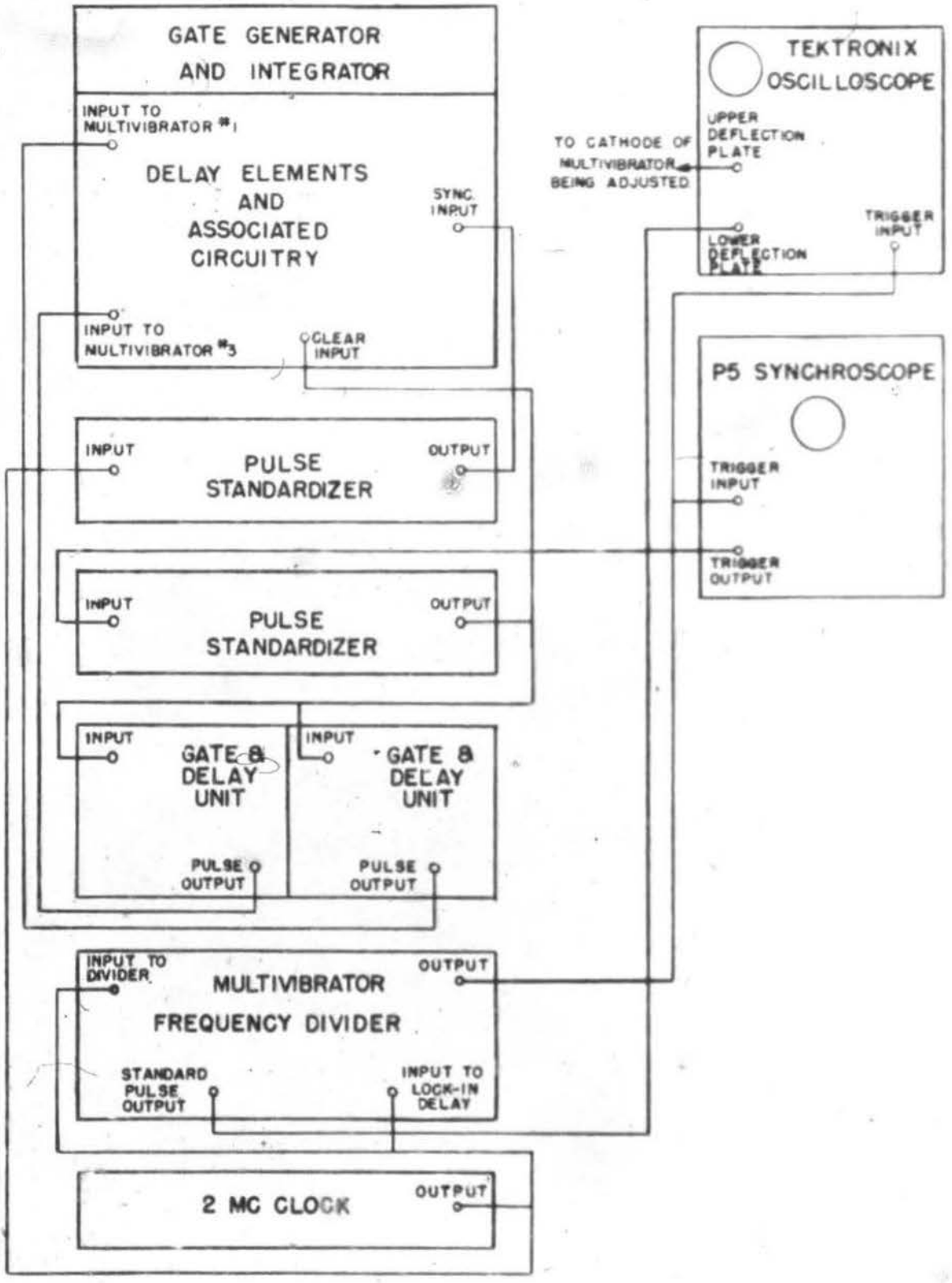
DEFLECTION SENSITIVITY: 60 VOLTS/INCH ON ALL PICTURES

FIG. 31



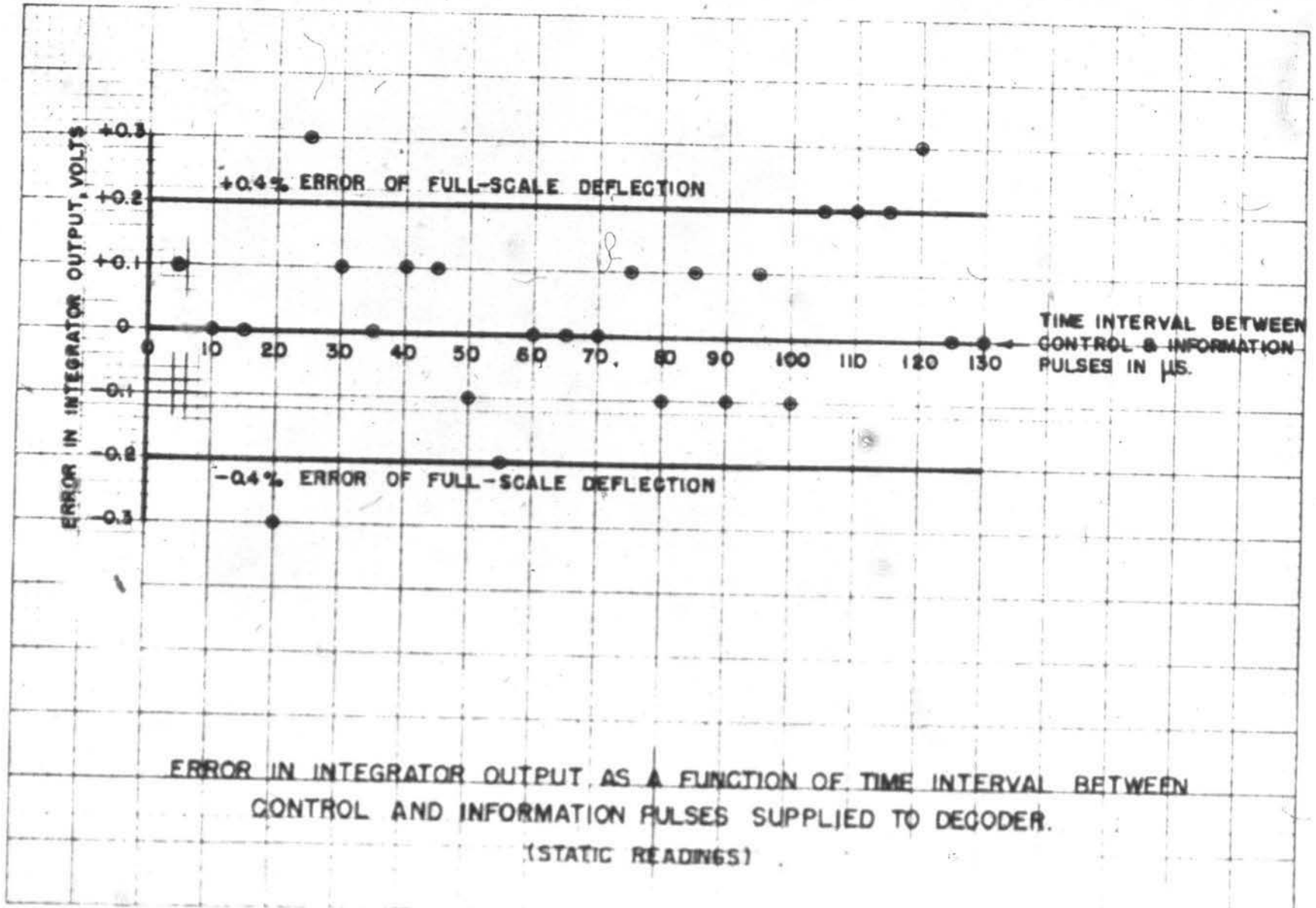
GATE GENERATOR AND INTEGRATOR

FIG. 32



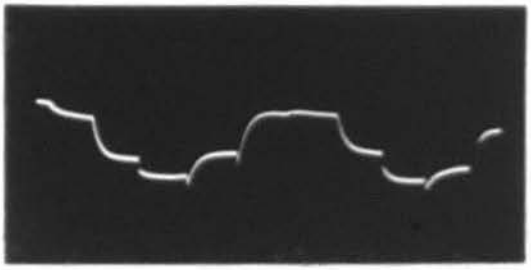
ARRANGEMENT OF TEST EQUIPMENT TO CALIBRATE
MULTIVIBRATORS 1, 2, 3, AND 4.

FIG 43

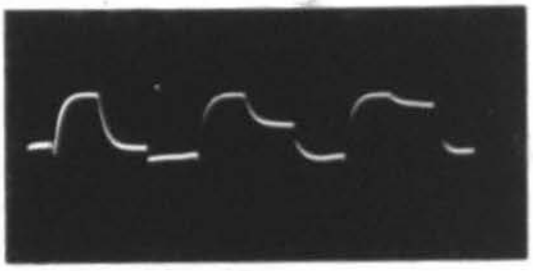


ERROR IN INTEGRATOR OUTPUT AS A FUNCTION OF TIME INTERVAL BETWEEN CONTROL AND INFORMATION PULSES SUPPLIED TO DECODER.

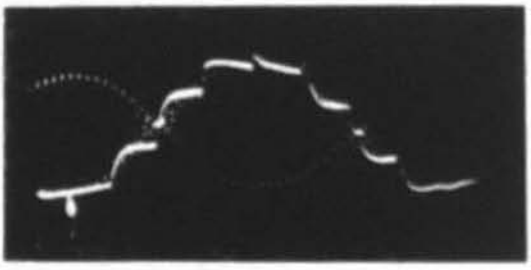
(STATIC READINGS)



OUTPUT OF DECODER FOR A SINUSOIDAL INPUT TO CODER OF 15 CPS



OUTPUT OF DECODER FOR A SINUSOIDAL INPUT TO CODER OF 25 CPS



SUPERPOSITION OF:

A. SINUSOIDAL INPUT TO CODER SHOWN AS MODULATION ON 1000 CPS SIGNAL

B. CORRESPONDING OUTPUT OF DECODER

SIGNAL FREQUENCY 10 CPS

FOR ALL PICTURES, THE SAMPLING RATE WAS APPROX. 100 SAMPLES PER SECOND.

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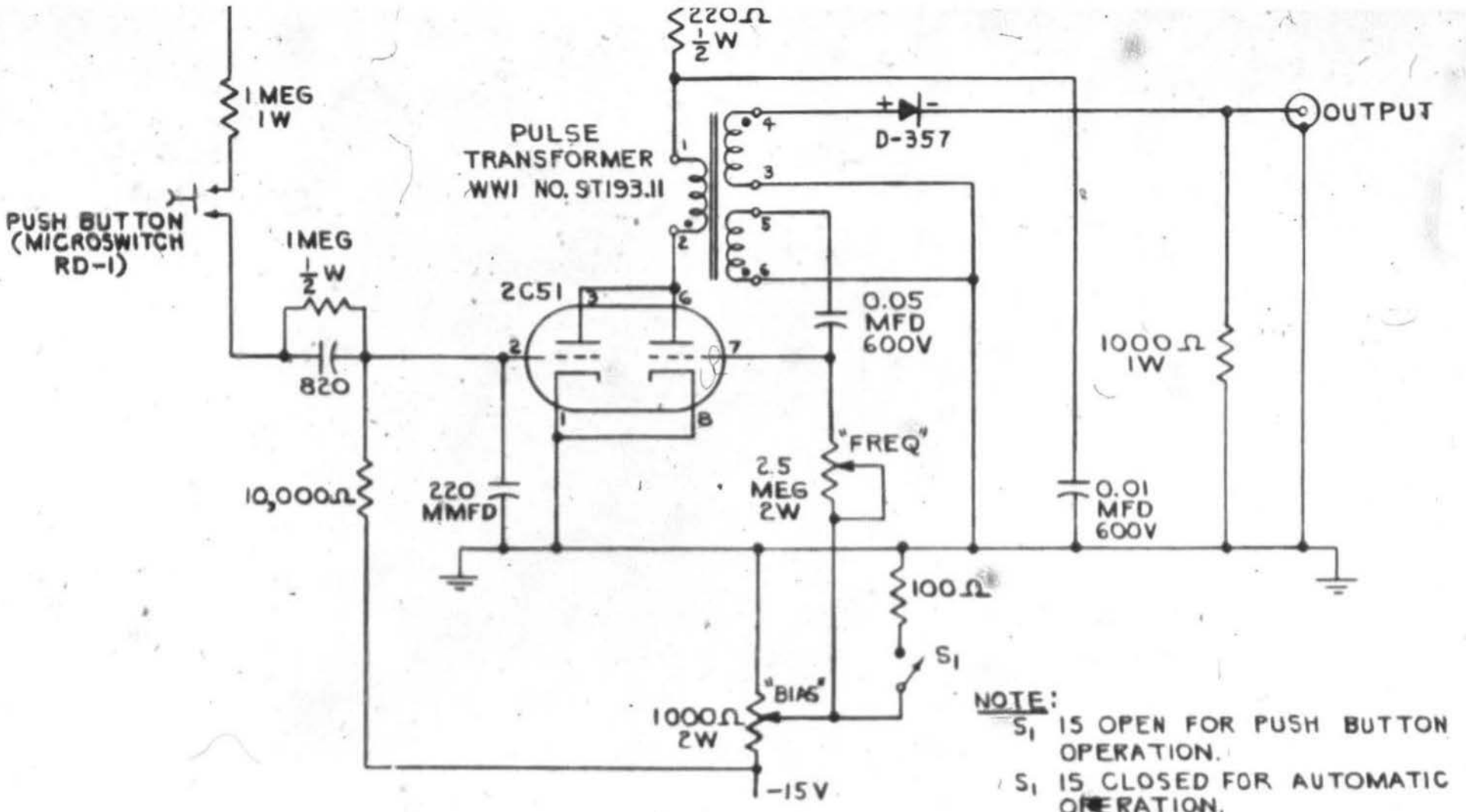

LOW-FREQUENCY BLOCKING OSCILLATOR

FIG. 36